AN2664
Application note

How to migrate from 70 nm to 57 nm technology in single level cell, large page, NAND flash memories

Introduction

The purpose of this application note is to give guidelines to migrate from the 70 nm to the 57 nm technology in single level cell (SLC), large page, NAND flash memory devices. In addition, the application note shows the advantages of the 57 nm technology over the 70 nm technology devices.

Section 1 and *Section 2* highlight the differences in commands and timings between 70 nm and 57 nm technology single level cell (SLC) NAND flash memories.

Section 3 explains how the differences between the two kinds of devices have an impact (in terms of hardware and software) on customer systems which include SLC large page NAND flash memories.

1 Commands

Table 1 shows the list of commands which are different for 70 nm and 57 nm SLC NAND flash memories. All other commands not listed in *Table 1* are the same for the two types of devices.

To make their systems work properly when replacing a 70 nm device with a new 57 nm device, customers must follow the information given in *Table 1*.

Table 1. Command set

Nr.	Command	57 nm technology	70 nm technology	Remark
1	Cache Read (sequential)	Yes	–	31h
2	Cache Read (device in 70 nm technology)	Yes	Yes	No added command
3	Cache Read (random) (device in 57 nm technology)	Yes	Yes	00h - 31h
4	Exit Cache Read	3Fh	34h	
5	Multiplane Page Program	Yes	–	
6	Copy Back Program	Yes*	Yes	*with Read EDC Status Register *same A18
7	Cache Program	–*	Yes	*Devices in 57 nm technology use the Multiplane Page Program command
8	Multiplane Copy Back Program	Yes	–	
9	Multiplane Block Erase	Yes	–	
10	Read Electronic Signature	Yes	Yes	4 read cycles (device in 70 nm) 5 read cycles (device in 57 nm)
11	Read Status Register	Yes	Yes	SR1 (cache program bit) is don't care on devices in 57 nm technology
12	Read Status Enhanced	Yes	–	
13	Read ONFI Signature	Yes	–	
14	Read Parameter Page	Yes	–	
15	Read EDC Status Register	Yes	–	
16	Read Block Lock Status	–	Yes*	*only 4-Gbit devices in 70 nm technology
17	Block Unlock	–	Yes*	*only 4-Gbit devices in 70 nm technology
18	Block Lock	–	Yes*	*only 4-Gbit devices in 70 nm technology
19	Block Lock-down	–	Yes*	*only 4-Gbit devices in 70 nm technology

2 Timings

Some AC characteristics and their values, improved in devices with 57 nm technology, are shown in *Table 2*.

Table 2. AC characteristics

Symbol	Alt. symbol		57 nm technology	4-Gbit, 70 nm technology	1/2-Gbit, 70 nm technology	Unit
t_{ALLWH}	t_{ALS}	Min	12	15	15	ns
t_{ALHWH}						
t_{CLHWH}	t_{CLS}	Min	12	15	15	ns
t_{CLLWH}						
t_{DVWH}	t_{DS}	Min	12	15	15	ns
t_{ELWH}	t_{CS}	Min	20	25	20	ns
t_{WLWH}	t_{WP}	Min	12	15	15	ns
t_{WLWL}	t_{WC}	Min	25(1)	30	30	ns
t_{ALLRL1}	t_{AR}	Min	10	15	10	ns
t_{ALLRL2}		Min	10	15	10	ns
t_{BLBH3}	t_{BERS}	Max	2	3	3	ms
t_{CLLRL}	t_{CLR}	Min	10	15	10	ns
t_{EHQZ}	t_{CHZ}	Max	30	50	30	ns
t_{RHQZ}	t_{RHZ}	Max	100	50	30	ns
t_{ELQV}	t_{CEA}	Max	25	30	25	ns
t_{EHQX}	$t_{OH}(t_{COH})$	Min	15	15	10	ns
t_{RLQX}	t_{RLOH}		5	–	–	ns
t_{RLRH}	t_{RP}	Min	12	15	15	ns
t_{RLRL}	t_{RC}	Min	25(1)	30	30	ns
t_{EHALX}	t_{CSD}	Min	10	–	–	ns
t_{EHCLX}						
t_{RLQV}	t_{REA}	Max	20	25	20	ns
t_{RHRL2}	t_{CRRH}	Min	-	100	–	ns
t_{RHWL}	t_{RHW}	Min	100	–	–	ns
t_{WHWH}	t_{ADL}	Min	70	100	100	ns

1. By upgrading to this timing, the throughput for read and write operations can be improved.

To obtain the best performances from SLC large page NAND flash memory devices, it is suggested aligning the timings with the values listed in the ‘57 nm technology’ column in *Table 2*.

3 Impact on software/hardware

3.1 Multiplane page program

SLC large page NAND flash memories in 57 nm technology do not feature cache program operation, which is replaced by multiplane page program operation. Customers only need to change their command set by using the multiplane page program instead of the cache program operation. The multiplane page program operation improves the cache program throughput by 30% for x8 devices and by 60% for x16 devices (see *Figure 1*, *Figure 2*, and *Figure 3*).

Customers who use the standard program operations do not need any changes in their command set.

Figure 1. Read performance evolution - 3 V, x8 devices

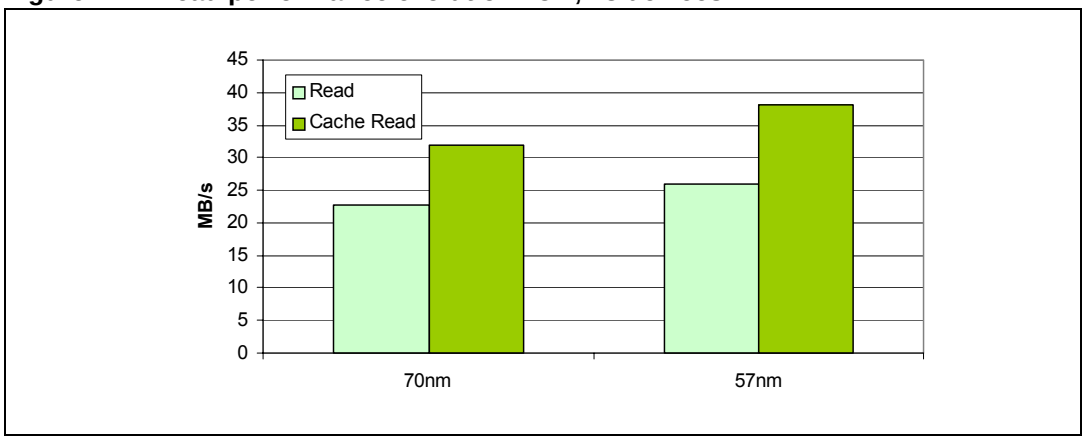


Figure 2. Program performance evolution - 3 V, x8 devices

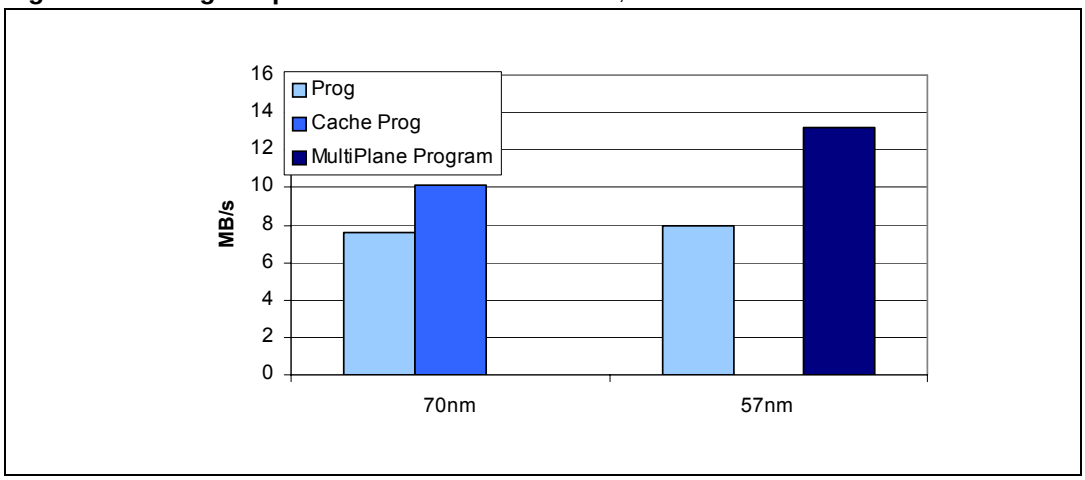
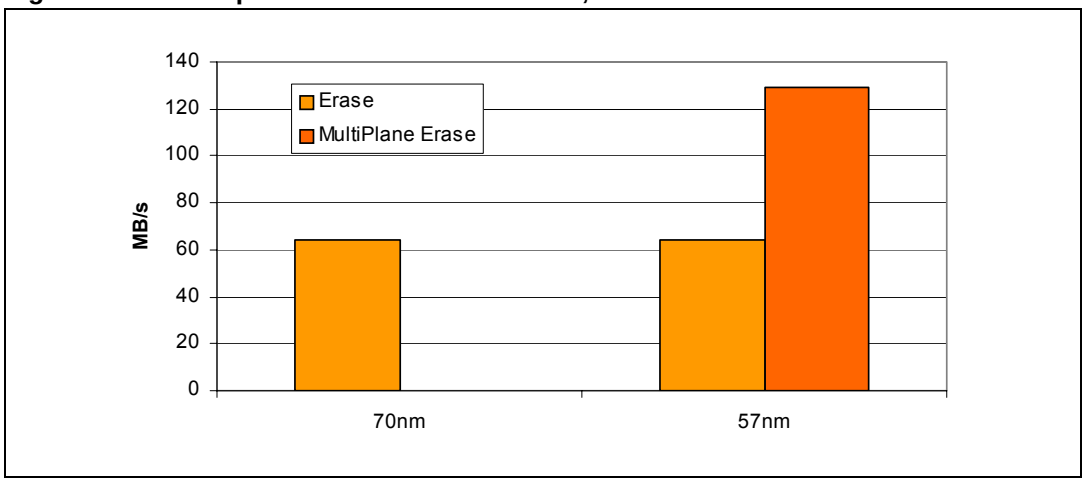


Figure 3. Erase performance evolution - 3 V, x8 devices



3.2 Compliancy with ONFI specification 1.0

Devices in 57 nm technology are compliant with ONFI specification 1.0. It is possible to use the ONFI commands in addition to the standard commands. Please refer to the datasheets of devices in 57 nm technology (see *Section 5: References*) for more details on ONFI sequences.

3.3 PRL pin in 70 nm technology, 4-Gbit memories

SLC large page NAND flash memories in 57 nm technology do not feature lock/unlock operations.

Among SLC large page NAND flash memory devices in 70 nm technology, only the 4-Gbit memory uses the Power-up Read Enable, Lock/Unlock (PRL) pin to enable and disable the lock mechanism. If customers in their systems use the PRL pin, nothing happens when replacing a 70 nm with a 57 nm device because this pin is left internally not connected.

3.4 Pin-to-pin compatibility

SLC large page NAND flash memories in 57 nm technology are pin-to-pin compatible with 70 nm devices. This means that customers do not need any hardware upgrade if the 70 nm and 57 nm devices are both available in the same package.

3.5 Multiplane copy back program operation

In 57 nm NAND flash memories, the copy back program operation is allowed only for pages of blocks that belong to the same plane. In other words, it is not possible to copy a page from a block belonging to the first plane in a block belonging to the second plane. For more details, please refer to the Section: Multiplane copy back program in the datasheets for devices in 57 nm technology.

4 Conclusions

NAND devices in 70 nm and 57 nm technology are pin-to-pin compatible, when delivered in the same packages.

All the features of the 70 nm SLC large page NAND flash memories are kept with the new 57 nm devices, except the cache program operation. Instead of the cache program, customers can adopt the multiplane page program operation, which also guarantees an improved program throughput. The Exit Cache Read command is changed to keep the ONFI compliancy (see *Exit Cache Read* in *Table 1: Command set*).

In 57 nm NAND flash memories, the copy back program operation is allowed only for pages of blocks that belong to the same plane.

Using standard operations, no change is required in the system software and the hardware remains the same thanks to pin-to-pin compatibility.

5 References

1. Devices in 70 nm technology:
   – NAND01G-B2B_NAND02G-B2C: 1-Gbit, 2-Gbit, 2112-byte/1056-word page, 1.8 V/3 V, NAND flash memory.
   – NAND04G-B2B_NAND08G-B2A: 4-Gbit, 8-Gbit, 2112-byte/1056-word page, 1.8 V/3 V supply voltage, NAND flash memory.
2. Devices in 57 nm technology:
   – NAND02G-B2D: 2-Gbit, 2112-byte/1056-word page, multiplane architecture, 1.8 V or 3 V, NAND flash memories.
   – NAND04G-B2D_NAND08G-BxC: 4-Gbit, 8-Gbit, 2112-byte/1056-word page, multiplane architecture, 1.8 V or 3 V, NAND flash memories.

6 Revision history

Table 3. Document revision history

Date	Revision	Changes
29-Nov-2007	1	Initial release.
04-Jan-2008	2	Applied Numonyx branding.
12-Jun-2008	3	Replaced ‘cache program’ with ‘70 nm technology’ and ‘multiplane page program’ with ‘57 nm technology’. Modified *Figure 1* and *Figure 2*. Added: *Figure 3*, *Section 3.2: Compliancy with ONFI specification 1.0*, *Section 3.5: Multiplane copy back program operation* and removed the Section on Exit Cache Read command.