
How to migrate from 70 nm to 48 nm technology
in 1-Gbit single level cell, large page, NAND flash memories

Introduction

The purpose of this application note is to give guidelines to migrate from the 70 nm to the 48 nm technology in 1-Gbit single level cell (SLC), large page, NAND flash memory devices.

[Section 1](#) and [Section 2](#) highlight the differences in commands and timings between 1-Gbit, 70 nm and 1-Gbit 48 nm technology single level cell (SLC) NAND flash memories.

[Section 3](#) explains how the differences between the two kinds of devices have an impact (in terms of hardware and software) on customer systems which include 1-Gbit SLC large page NAND flash memories.

1 Commands

[Table 1](#) shows a command set comparison between 1-Gbit SLC NAND flash memories in 70 nm technology and 48 nm technology.

Table 1. Command set

Command	48 nm technology (NAND01G-B2C)	70 nm technology (NAND01G-B2B)
Read	00h 30h	00h 30h
Random Data Output	05h E0h	05h E0h
Cache Read	00h 31h	00h 31h
Exit Cache Read	3Fh	34h
Page Program	80h 10h	80h 10h
Random Data Input	85h	85h
Copy Back Program	00h 35h 85h 10h	00h 35h 85h 10h
Cache Program	Not supported	80h 15h
Block Erase	60h D0h	60h D0h
Reset	FFh	FFh
Read Electronic Signature	90h	90h
Read Status Register	70h	70h
Read ONFI Parameter Page	ECh	Not supported

2 Timings

[Table 2](#) shows a comparison of AC characteristics between devices in 70 nm and devices in 48 nm technology.

Table 2. AC characteristics

Symbol	Alt. symbol		48 nm technology (NAND01G-B2C)		70 nm technology (NAND01G-B2B)		Unit
			1.8 V	3.0 V	1.8 V	3.0 V	
t_{ALLWH}	t_{ALS}	Min	25	12	25	15	ns
t_{ALHWH}							
t_{CLHWH}	t_{CLS}	Min	25	12	25	15	ns
t_{CLLWH}							
t_{DVWH}	t_{DS}	Min	20	12	20	15	ns
t_{ELWH}	t_{CS}	Min	35	20	35	20	ns
t_{WHALH}	t_{ALH}	Min	10	5	10	5	ns
t_{WHALL}							
t_{WHCLH}	t_{CLH}	Min	10	5	10	5	ns
t_{WHCLL}							
t_{WHDX}	t_{DH}	Min	10	5	10	5	ns
t_{WHEH}	t_{CH}	Min	10	5	10	5	ns
t_{WHWL}	t_{WH}	Min	15	10	15	10	ns
t_{WLWH}	t_{WP}	Min	25	12	25	15	ns
t_{WLWL}	t_{WC}	Min	45	25	45	30	ns
t_{ALLRL1}	t_{AR}	Min	10	10	10	10	ns
t_{ALLRL2}							
t_{BHRL}	t_{RR}	Min	20	20	20	20	ns
t_{BLBHx}		Typ	3	3	–	–	μ s
		Max	25	25	–	–	
t_{BLBH1}		Max	25	25	25	25	μ s
t_{BLBH2}	t_{PROG}	Max	700	700	700	700	μ s
t_{BLBH3}	t_{BERS}	Max	3	3	3	3	ms
t_{BLBH4}	t_{RST}	Ready/Read	Max	5	5	5	μ s
		Program		10	10	10	
		Erase		500	500	500	
t_{BLBH5}	t_{CBSY}	Typ	–	–	3	3	μ s
		Max	–	–	700	700	

Table 2. AC characteristics (continued)

Symbol	Alt. symbol		48 nm technology (NAND01G-B2C)		70 nm technology (NAND01G-B2B)		Unit
			1.8 V	3.0 V	1.8 V	3.0 V	
t _{CLLRL}	t _{CLR}	Min	10	10	10	10	ns
t _{DZRL}	t _{IR}	Min	0	0	0	0	ns
t _{EHQZ}	t _{CHZ}	Min	30	30	30	30	ns
t _{RHQZ}	t _{RHZ}	Max	100	100	30	30	ns
t _{WHWH}	t _{ADL}	Min	100	70	100	100	ns
t _{VHWH}	t _{WW}	Min	100	100	100	100	ns
t _{VLWH}							
t _{ELQV}	t _{CEA}	Max	45	25	45	25	ns
t _{RHRL}	t _{REH}	Min	15	10	15	10	ns
t _{EHQX}	t _{OH}	Min	15	15	10	10	ns
t _{RHQX}							
t _{RLQX}	t _{RLOH}		–	5	–	–	ns
t _{RLRH}	t _{RP}	Min	25	12	25	15	ns
t _{RLRL}	t _{RC}	Min	45	25	50	30	ns
t _{RLQV}	t _{REA}	Max	30	20	30	20	ns
t _{WHBH}	t _R	Max	25	25	25	25	μs
t _{WHBL}	t _{WB}	Max	100	100	100	100	ns
t _{WHRL}	t _{WHR}	Min	60	60	60	60	ns
t _{EHALX}	t _{CSD}	Min	10	10	–	–	ns
t _{EHCLX}							
t _{RHWL}	t _{RHW}	Min	100	100	–	–	ns

3 Impact on software/hardware

3.1 Cache program

The cache program operation is not supported in 1-Gbit SLC large page NAND devices in 48 nm technology. Customers have to use the standard page program operation.

For performance comparison between 1-Gbit devices in 70 nm and 48 nm technology, please refer to the [Section 3.5](#).

3.2 Cache read

1-Gbit devices in 48 nm technology implement a new cache read sequence, compliant with ONFI 1.0 specification.

[Figure 1](#) and [Figure 2](#) show the cache read sequence supported by 1-Gbit SLC large page NAND devices in 70 nm and 48 nm technology, respectively.

Figure 1. Cache read operation in 70 nm technology, 1-Gbit devices

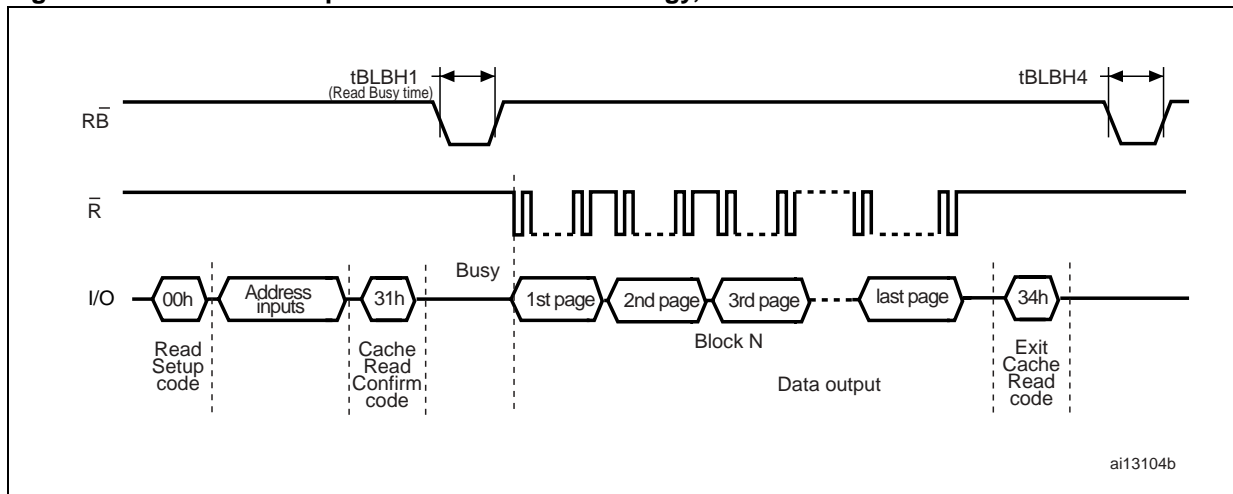
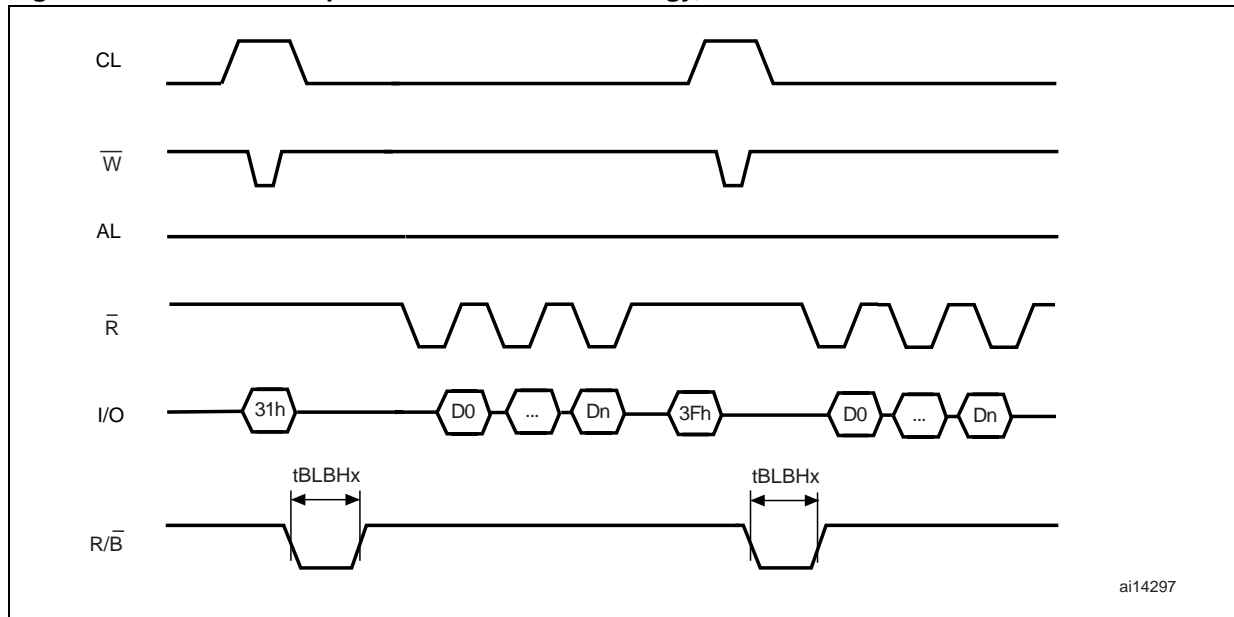


Figure 2. Cache read operation in 48 nm technology, 1-Gbit devices



3.3 Page program

In 1-Gbit SLC large page devices in 48 nm technology the pages within a given block must be programmed sequentially.

3.4 Pin-to-pin compatibility

1-Gbit SLC large page NAND flash memories in 48 nm technology are pin-to-pin compatible with 70 nm 1-Gbit devices. This means that customers do not need any hardware upgrade if the 70 nm and 48 nm devices are both available in the same package.

3.5 Performance comparison

Figure 3, Figure 4, and Figure 5 show a performance comparison between the 1-Gbit device in 70 nm technology (NAND01G-B2B) and the 1-Gbit device in 48 nm technology (NAND01G-B2C), without considering host overhead.

As shown, read performance can be improved using new timings while the lack of cache program is partially recovered by the timings improvement, which characterizes the 1-Gbit device in 48 nm technology.

Figure 3. Read performance evolution - 3 V, x8 devices

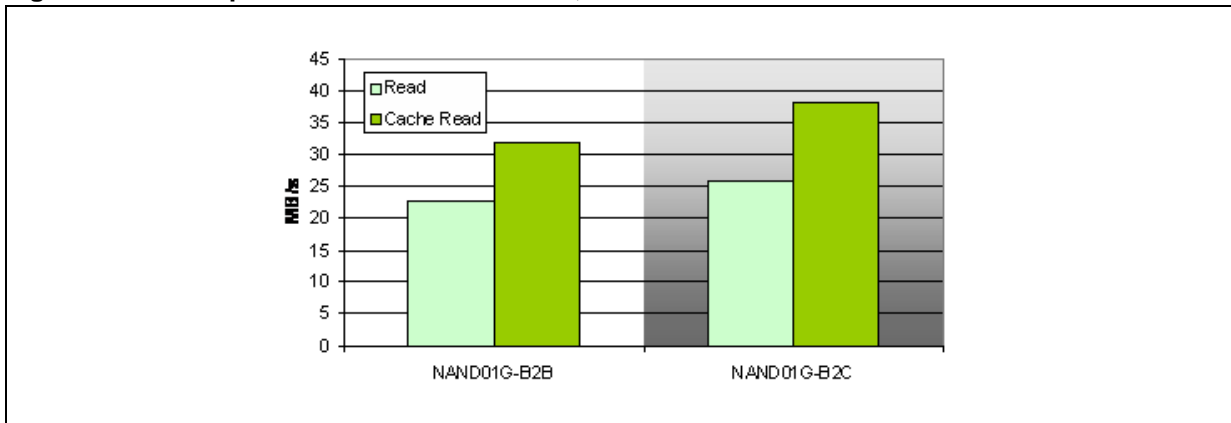


Figure 4. Program performance evolution - 3 V, x8 devices

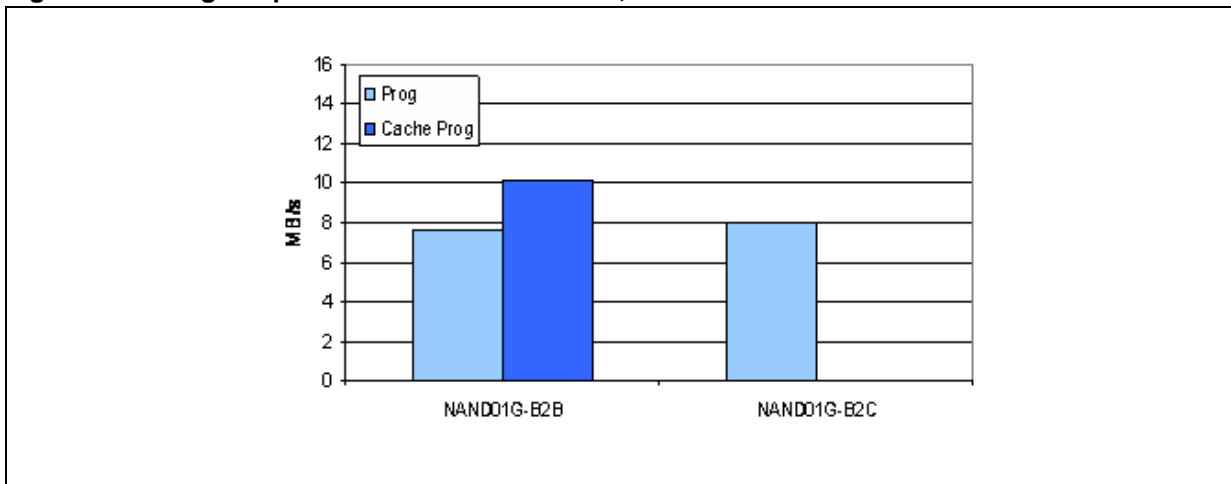
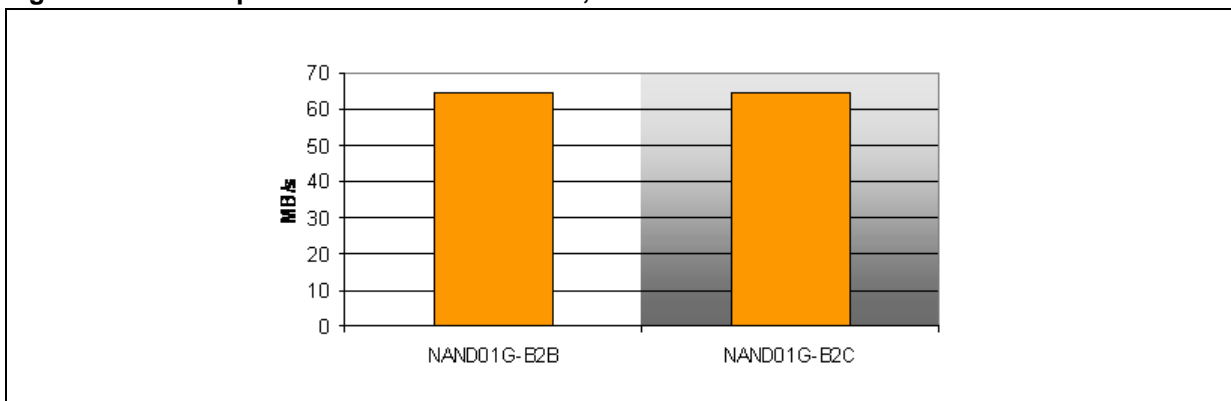


Figure 5. Erase performance evolution - 3 V, x8 devices



4 Conclusions

1-Gbit SLC large page NAND devices in 70 nm and 48 nm technology are pin-to-pin compatible, when delivered in the same packages.

All the features of the 70 nm 1-Gbit SLC large page NAND flash memories are kept with the new 48 nm devices, except the cache program operation. The lack of the cache program operation in 48 nm devices is partially covered by timings improvement. The Exit Cache Read command is changed to keep the ONFI compliancy (see [Exit Cache Read](#) in [Table 1: Command set](#)).

Using standard operations, no change is required in the system software and the hardware remains the same thanks to pin-to-pin compatibility.

When using cache program and cache read operations, the system software must be changed as explained in [Section 3.1: Cache program](#) and [Section 3.2: Cache read](#).

5 References

1. 1-Gbit SLC large page devices in 70 nm technology:
 - NAND01G-B2B_NAND02G-B2C: 1-Gbit, 2-Gbit, 2112-byte/1056-word page, 1.8 V/3 V, NAND flash memory.
2. 1-Gbit SLC large page devices in 48 nm technology:
 - NAND01G-B2C: 1-Gbit, 2112-byte/1056-word page, 1.8 V/3 V, NAND flash memory.

6 Revision history

Table 3. Document revision history

Date	Revision	Changes
24-Jun-2008	1	Initial release.
12-Dec-2008	2	Added Section 3.3: Page program .

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