

Customer Service Note

Lead Frame Package User Guidelines

Introduction

When size constraints allow, the larger-pitched lead-frame-based package design can provide the simplest surface mount technology (SMT) integration solution. The maturity and reliability of lead frame packaging can make it the best choice for lower die count, lower I/O count, and less space-constrained and/or lower-cost applications.

This document is intended as a customer's user guide to provide high-level information related to the lead frame packages produced by Micron. It will discuss package types, frame finishes used in the industry, and various soldering process methods and related issues.

For additional information and assistance for any manufacturability issues, see www.micron.com.

Micron Lead Frame Package Options

Table 1: Micron Lead Frame Packages

Interface	Package Type	Number of Pads/Balls/Leads	Size (mm)	Notes
Parallel	TSOP	48	12 x 20	1
		56	14 x 20	
	PLCC	32	11.48 x 14.2	
	SSOP	44	28.2 x 16	
Serial	SOIC 8N	8	6 x 5	
	SOIC 8W	8	6 x 6.2	
	SOIC 16W	16	10.5 x 7.6	
	DFN-8	-	2 x 3, 4 x 3, 5 x 6, 6 x 8	1
	TSSOP8	8	4.4 x 6.4	
	PDIP	8	9.2 x 7.87	
Automotive	TSOP	48	12 x 20	
		56	14 x 20	
	SOIC 8N	8	6 x 5	
	SOIC 8W	8	6 x 6.2	
	SOIC 16W	16	10.5 x 7.6	
	SSOP	44	28.2 x 16	
	PQFP80	80	14 x 20	

Notes: 1. Other package sizes and signal pitches may be available; contact your Micron representative for more information.

Micron is moving toward eliminating lead (Pb) from packages in accordance with RoHS standards and Waste Electrical and Electronics Equipment (WEEE) international regulations. Our current proportion of Pb-free to Pb-containing lead frame packages is 97% and 3%, respectively. Most of our customers have successfully adopted Pb-free lead frame packages.

Pb-Free Lead Frame Finishes

Micron Pb-free packages have a matte tin finish or NiPdAu, preplated frame (PPF) finish, depending on the manufacturing site. Matte tin is considered the industry standard. Micron's typical PPF file nominal thicknesses are:

- Au ~ 0.003 μ m to 0.012 μ m
- Pd ~ 0.03 μ m to 0.11 μ m
- Ni ~ 0.5 μ m to 1.2 μ m

NiPdAu Finish/Solder Compatibility

- Components with NiPdAu (or matte tin) finishes can withstand much higher soldering temperatures than some other tin/lead finished packages.
- Paste application and component placement do not require specific actions.
- During reflow, protective layers of Au and Pd are dissolved into the solder.
- A thin SiNi IMC layer is observed after reflow.
- Thermal cycling test results indicate that NiPdAu surface finish and matte tin finish packages have similar solder joint reliability.

Stenciling

Aperture Size vs. Board Land Size for Pb-Free Solder Paste

Generally, the aperture size of the stencil should be very close to 1:1 compared to the board land size. This is done to ensure complete coverage of the land with solder after reflow.

Some slight reduction (~0.013mm) per side of the land is acceptable because pushing the component into the solder paste will cause the paste to spread and cover the land. A reduction of the aperture size for the ground plane of QFN or LCC devices is a desirable exception. Radius corners are also acceptable because solder paste is more likely to stick to apertures with sharp corners.

For surface mount devices (SMDs) with leads, for example, J-leaded or gull-wing components with 1.3–0.4mm (51.2–15.7 mil) pitch, the reduction is typically 0.254mm (1.0 mil) in width and no reduction in length.

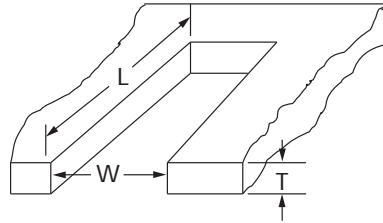
Aperture Size vs. Board Land Size for Tin/Lead Solder Paste

Generally, the aperture size of the stencil should be reduced compared to the board land size. The stencil is usually modified with respect to the original land design.

Reduced stencil design areas and changes to aperture shapes are desirable to improve the processes of printing, reflow, or stencil cleaning. A smaller aperture will decrease the stencil-to-board land alignment. Radiused aperture corners will improve stencil cleaning.

For SMDs with leads, for example, J-lead or gull-wing components with 0.4–1.3mm (15.7–51.2 mil) pitch, the reduction is typically 0.05–0.08mm (1.2–3.1 mil) in width and 0.05–0.13mm (2.0–5.1 mil) in length.

Figure 1: Cross-Sectional View of a Stencil



$$\text{Aspect ratio} = \frac{\text{Width of aperture}}{\text{Thickness of stencil}} = \frac{W}{T}$$

$$\text{Area ratio} = \frac{\text{Area of aperture}}{\text{Area of aperture walls}} = \frac{L \times W}{2 \times (L + W) \times T}$$

For detailed stenciling information, see IPC-7525A “Stencil Design Guidelines,” and IPC-7526 “Stencil and Misprinted Board Cleaning Handbook.”

Package-to-Board Assembly Process

Process Differences for Various Lead-Frame Finishes

- For copper lead frames with an NiPdAu coating, the soldering process includes wetting the surface of the board with molten solder, dissolving Pd and Au thin layers in the solder, and creating an SnNi intermetallic layer by diffusion.
- For copper and alloy 42 lead frames with tin coating or tin/lead finish, the soldering process includes melting the solder paste, wetting the tin coated connection, and, as a result of the quick diffusion process, melting the coating layer, and then soldering by diffusion, which creates an intermetallic layer (NiSn or CuSn).

The preheating and the length of the typical convection reflow profile result in no major differences when soldering tin-plated or tin/lead-plated components.

Solder Paste

The main components of solder paste are 80–95% solder powder (by weight) and flux. The amount of solder powder determines the viscosity and thickness of solder after reflow. The particle size of the solder paste effects the printing capabilities of the paste, and the spherical-shaped particles are used for the finer-pitched package applications. Flux is used to remove oxidized matter from solder surfaces, prevent re-oxidation during the soldering process, and reduce surface tension of molten solder.

Most paste manufacturers provide a suggested thermal profile for their products; these should be referenced prior to manufacturing.

Micron has experienced excellent surface mount results using low residue, no-clean solder paste (flux class ROL 0 per J-STD-004, Alloy SAC 305 or 405 with 89% metal content).

Lead-Frame Package Soldering Processes

The two types of soldering processes are partial heating methods, which apply heat to the package leads and/or PCB in localized areas, and total heating methods, which apply heat to the entire package and PCB.

Partial heating methods can cause less thermal stress to the component and PCB, which is beneficial for components with low heat resistance, but these methods are not compatible for high volume production. Total heating methods are repeatable, low cost per unit, and widely used in the industry, but these methods apply more thermal stress to the total package and PCB when compared to partial heat methods.

Micron does not recommend any specific process; customers must select the best process for their components, package type, and application.

The following table lists the various process methodologies and their advantages and disadvantages.

Table 2: Partial vs. Total Heating Soldering Methods

Soldering Method	Advantages	Disadvantages		
Partial (Local) Heating				
Soldering iron	<ul style="list-style-type: none"> Low thermal stress 	<ul style="list-style-type: none"> Large temperature variations High operating costs 		
Hot air	<ul style="list-style-type: none"> Low thermal stress 	<ul style="list-style-type: none"> Large temperature variations High operating costs 		
Laser	<ul style="list-style-type: none"> Low thermal stress Post-soldering is possible 	<ul style="list-style-type: none"> Long processing times, not practical for mass production All leads and components must be heated 		
Pulse heating	<ul style="list-style-type: none"> Low thermal stress Post-soldering is possible 	<ul style="list-style-type: none"> Long processing times, not practical for mass production All leads and components must be heated 		
Total Heating				
Infrared (IR reflow)	<ul style="list-style-type: none"> Low operating costs Short processing times Simple structures 	<ul style="list-style-type: none"> Large temperature variations High thermal stress Difficulty heating components in shadows Component shapes and colors can cause temperature variations (for near-IR) 		
Convection (convection reflow)	<ul style="list-style-type: none"> Medium temperature variations Easy to apply direct heat to high-density parts and to parts in shadows Even heating is possible Possible to attain even heat distribution on boards and components that have different thermal capacities 	<ul style="list-style-type: none"> High thermal stress Longer processing times compared to IR reflow Flow speed can cause component displacement and board vibrations 		
	Air		<ul style="list-style-type: none"> Low operating costs 	<ul style="list-style-type: none"> Solder defects can be caused by copper foil oxidation
	N2		<ul style="list-style-type: none"> Low incidence of solder defects caused by copper foil oxidation 	<ul style="list-style-type: none"> High operating costs

Table 2: Partial vs. Total Heating Soldering Methods (Continued)

Soldering Method	Advantages	Disadvantages	
Combined IR/ convection	<ul style="list-style-type: none"> • Medium temperature variations • Short processing times • Easy to apply direct heat to high-density parts and to parts in shadows • Even heating is possible • Possible to attain even heat distribution on boards and components that have different thermal capacities 	<ul style="list-style-type: none"> • High thermal stress • Flow speed can cause component displacement and board vibrations • Solder defects can be casued by copper foil oxidation (on convection reflow) 	
	Air	<ul style="list-style-type: none"> • Low operating costs 	<ul style="list-style-type: none"> • Solder defects can be casued by copper foil oxidation
	N2	<ul style="list-style-type: none"> • Low incidence of solder defects caused by copper foil oxidation 	<ul style="list-style-type: none"> • High operating costs
Vapor phase soldering (VPS)	<ul style="list-style-type: none"> • Small temperature variations • Precise temperature control is possible • No temperature control system is required • Lower heating times and temperatures are possible • Minimal oxidation and contamination of soldered sections 	<ul style="list-style-type: none"> • High thermal stress • High operating costs • High equipment costs 	
Flow (wave) soldering	<ul style="list-style-type: none"> • Low thermal stress • Low processing times • Low thermal stress (THD) 	<ul style="list-style-type: none"> • Large temperature variations • Difficulty handling diverse package types • High thermal stress (SMD) 	

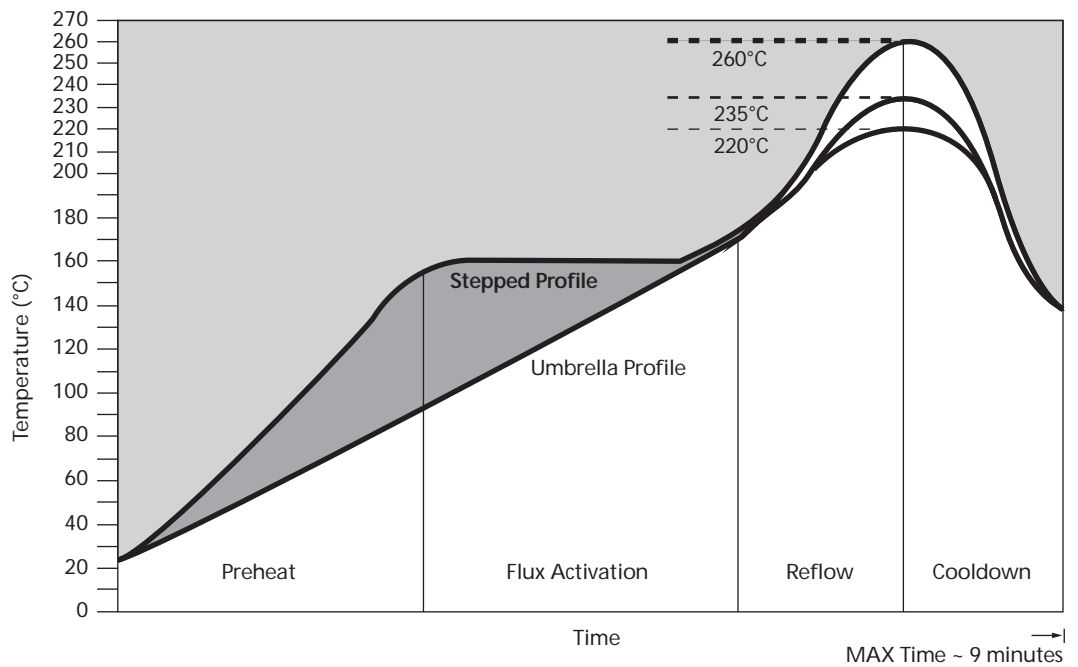
Reflow Profile (Total Heating)

The table and figure below depict general reflow information. Refer to Micron technical note TN-00-15, Recommended Soldering Parameters, for more details on SMT reflow parameters.

Table 3: Minimum and Recommended Profiles for Convection Reflow Soldering

Convection Reflow Profile	Minimum Peak Temperature	Minimum Time Above Liquidus of Solder Paste Materials	Recommended Peak Temperature and Time Above Liquidus
Lead solders (SnPb)	210°C	20 seconds	220°C – 30 seconds
Pb-free solders (SnAgCu)	235°C	20 seconds	245°C – 30 seconds

Figure 2: Minimum and Maximum Reflow Temperatures

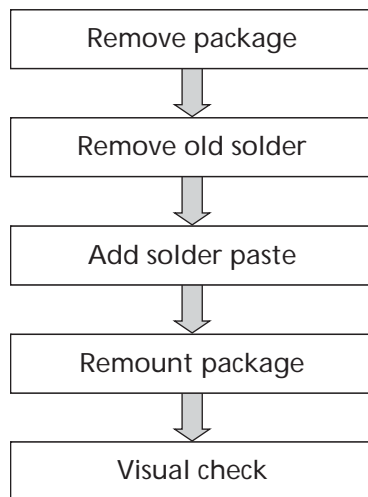


Rework Process Considerations

There are several methods used to rework components, including solder iron, hot air soldering, laser, pulse, and the reflow processes that were described earlier. The maximum number of reflows or thermal cycles is defined as three; reworking may exceed this limit, but, if it does, product guarantees may be invalidated. We strongly recommend component reuse be avoided.

The rework process method varies by device type and application (SMD, THD, and so on), but the basic process flow is outlined below.

Figure 3: Rework Process Flow





Micron lead-frame package storage and handling conditions are based on JEDEC Standards J-STD-033B.1 and J-STD-020D0.01. See technical note TN-00-01, *Moisture Sensitivity of Plastic Packages*, for additional information on allowable environmental exposure prior to reflow processing.

For signal integrity information, see technical note TN-00-20, *Understanding the Value of SI Testing*.

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Revision History

Rev. A	5/11
• Initial release	