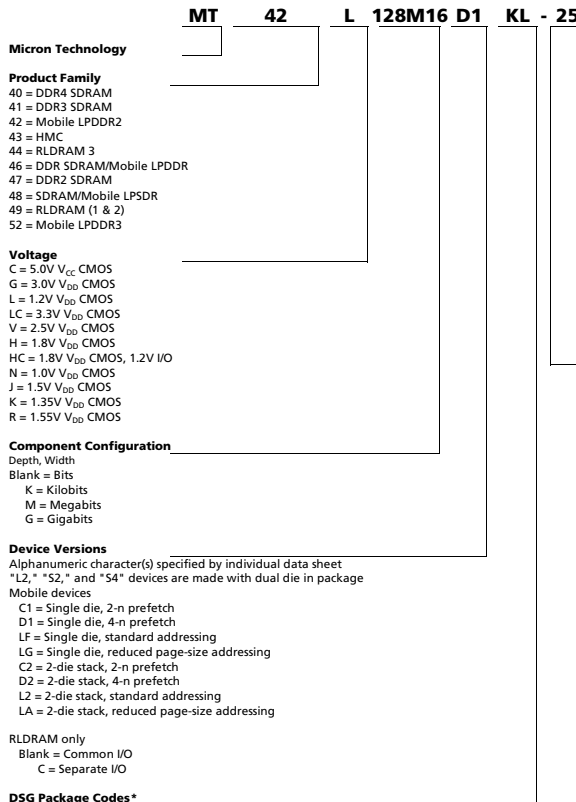


# DRAM Component Part Numbering System

The part numbering system is available at [www.micron.com/numbering](http://www.micron.com/numbering)

## DDR4/DDR3/DDR2/DDR/SDRAM, Mobile LPDDR2/LPDDR/LPSDR, and RLD RAM® Memory



### Die Revision Designator

### Special Processing

ES = Engineering sample  
 Blank = Production

### Operating Temperatures

Blank = Commercial temperature  
 IT/AIT\*\* = Industrial temperature  
 AT/AAT = Automotive temperature

\*\*The number one (1) and the capital letter "I" utilize the same laser mark—"I1"

### Special Options

(Multiple processing codes are separated by a space and are listed in hierarchical order)  
 L = Low power  
 M = Reduced IDD6

### Access/Cycle Time

DRAM Technology	Speed Grade Mark	t <sub>RAC</sub> Access Time
All DRAM	-0	Untested
	-A	Untested

DRAM Technology	Speed Grade Mark	MAX Clock Frequency	PC Targets CL <sup>1</sup> RCD <sup>2</sup> RP
DDR4 SDRAM	-125	800 MHz	11-11-11
	-107	933 MHz	13-13-13
	-107H	933 MHz	14-13-13
	-093	1067 MHz	14-14-14
	-093H	1067 MHz	15-14-14
	-083	1200 MHz	16-16-16
	-083	1200 MHz	16-16-16
DDR3 SDRAM	-25	400 MHz	6-6-6
	-25E	400 MHz	5-5-5
	-187	533 MHz	8-8-8
	-187E	533 MHz	7-7-7
	-187F	533 MHz	6-6-6
	-15	667 MHz	10-10-10
	-15E	667 MHz	9-9-9
	-15F	667 MHz	8-8-8
	-15H	667 MHz	10-9-9
	-125	800 MHz	11-11-11
	-125E	800 MHz	10-10-10
	-125H	800 MHz	12-11-11
DDR2 SDRAM	-107	933 MHz	13-13-13
	-107H	933 MHz	14-13-13
	-093	1067 MHz	14-14-14
	-5E	200 MHz	3-3-3
	-37E	267 MHz	4-4-4
	-3	333 MHz	5-5-5
DDR SDRAM	-3E	333 MHz	4-4-4
	-25	400 MHz	6-6-6
	-25E	400 MHz	5-5-5
	-187E	533 MHz	7-7-7
	-75	133 MHz	2-5-3
SDRAM	-6T	167 MHz	2-5-3
	-6	167 MHz	2-5-3
	-5B	200 MHz	3-3-3
	-75	133 MHz	3-3-3
	-7E	133 MHz	2-2-2
Mobile LPDDR2	-7	143 MHz	3-3-3
	-6	167 MHz	3-3-3
	-6A	167 MHz	3-3-3
	-55	183 MHz	3-3-3
	-5	200 MHz	3-3-3
Mobile LPDDR	-18	533 MHz	
	-25	400 MHz	
	-3	333 MHz	
	-37	266 MHz	
	-5	200 MHz	
Mobile LPSDR	-75	133 MHz	
	-6	167 MHz	
	-54	185 MHz	
	-5	200 MHz	
	RLDRAM 1 & 2	-8	125 MHz
-75		133 MHz	
-6		167 MHz	
-5		200 MHz	
-33		300 MHz	
RLDRAM 3	-25	400 MHz with t <sub>RC</sub> 20ns	
	-25E	400 MHz with t <sub>RC</sub> 15ns	
	-18	533 MHz	
	-125	800 MHz with t <sub>RC</sub> (MIN) 12ns	
	-125E	800 MHz with t <sub>RC</sub> (MIN) 10ns	
Mobile Package Codes*	-107	933 MHz with t <sub>RC</sub> (MIN) 10ns	
	-107E	933 MHz with t <sub>RC</sub> (MIN) 8ns	
	-093	1067 MHz with t <sub>RC</sub> (MIN) 10ns	
	-093E	1067 MHz with t <sub>RC</sub> (MIN) 8ns	
	-093E	1067 MHz with t <sub>RC</sub> (MIN) 8ns	

Lead Plating	Pb-Free/RoHS-Compliant Plating	Package Description***
<b>DDR4 SDRAM</b>		
-	HA	FBGA (96-ball, 9 x 14)
-	HX	FBGA (78-ball, 9 x 11.5)
-	TRF	FBGA (TwinDie, 78-ball, 9.5 x 11.5)
<b>DDR3 SDRAM</b>		
-	DA	FBGA (78-ball, 8 x 10.5)
-	HA	FBGA (96-ball, 9 x 14)
-	HX	FBGA (78-ball, 9 x 11.5)
-	JP	FBGA (78-ball, 8 x 11.5)
-	JT	FBGA (96-ball, 8 x 14)
-	RA	FBGA (78-ball, 10.5 x 12)
-	RE	FBGA (96-ball, 10 x 14)
-	RH	FBGA (78-ball, 9 x 10.5)
-	SHM	FBGA (QuadDie, 78-ball, 10.5 x 12)
-	STA	FBGA (QuadDie, 3DS, 78-ball, 10.5 x 12)
-	SMA	FBGA (QuadDie, 78-ball, 9.5 x 11.5)
-	SLD	FBGA (TwinDie, 136-ball, 10 x 14)
-	THD	FBGA (TwinDie, 78-ball, 9 x 11.5 x 1.2)
-	THE	FBGA (TwinDie, 78-ball, 10.5 x 12)
-	THG	FBGA (TwinDie, 3DS, 78-ball, 10.5 x 12)
-	THV	FBGA (TwinDie, 78-ball, 8 x 11.5)
-	THA	FBGA (QuadDie, 78-ball, 10 x 11.5)
-	TNA	FBGA (TwinDie, 96-ball, 10x14 X8+X8)
-	THW	FBGA (QuadDie, 78-ball, 8 x 11.5)
-	TRF	FBGA (TwinDie, 78-ball, 9.5 x 11.5)
<b>DDR2 SDRAM</b>		
-	BP	FBGA (60-ball, 8 x 12)
-	BG	FBGA (84-ball, 8 x 14)
-	JN	FBGA (60-ball, 8 x 10)
-	HR	FBGA (84-ball, 8 x 12.5)
-	B6	FBGA (60-ball, 10 x 10)
-	BN	FBGA (84-ball, 10 x 12.5)
-	HV	FBGA (60-ball, 8 x 11.5)
-	HR	FBGA (84-ball, 8 x 12.5)
-	RT	FBGA (84-ball, 9 x 12.5)
-	HG	FBGA (60-ball, 84-ball, 11.5 x 14)
-	EB	FBGA (60-ball, 9 x 11.5)
-	WTR	FBGA (TwinDie, 63-ball, 9 x 11.5)
-	THM	FBGA (TwinDie, 63-ball, 12 x 14)
-	THN	FBGA (TwinDie, 63-ball, 9 x 11.5)
-	THN	FBGA (TwinDie, 63-ball, 8 x 10 [1Gb-50nm only])
-	WTR	FBGA (TwinDie, 63-ball, 9 x 11.5)
-	THT	FBGA (Quad die, 65-ball, 9 x 11.5)
<b>DDR SDRAM</b>		
-	CY	FBGA (84-ball, 60-ball, 8 x 12.5)
-	BG	FBGA (84-ball, 60-ball, 8 x 14)
-	BN	FBGA (54-ball, 60-ball, 84-ball, 10 x 12.5)
-	TG	TSOP (Type II)
<b>SDRAM</b>		
-	BB	FBGA (60-ball, 8 x 16)
-	BG	VFPGA (54-ball), FBGA (84-ball, 60-ball, 8 x 14)
-	B4	VFPGA (54-ball, 8 x 8)
-	B5	VFPGA (90-ball, 8 x 13)
-	P	TSOP (Type II)
-	xT	Stacked TSOP, "x" = internal stacking code
<b>RLDRAM 1 &amp; 2</b>		
-	BM	µBGA (144-ball, 11 x 18.5)
-	HT	FBGA (144-ball, 11 x 18.5)
<b>RLDRAM 3</b>		
-	PA	FBGA (168/169-ball, 13.5 x 13.5 x 1.2) SDP
-	PKM	FBGA (168/169-ball, 13.5 x 13.5 x 1.45) DDP

### Mobile Package Codes\*

Lead Plating	Pb-Free/RoHS-Compliant Plating	Package Description***
<b>Mobile LPDDR2</b>		
-	KF	PoP (136-ball, 10 x 10)
-	KH	PoP (216-ball, 12 x 12)
-	KJ	PoP (216-ball, 12 x 12)
-	KL	PoP (168-ball, 12 x 12)
<b>Mobile LPDDR</b>		
-	BF	VFPGA (60-ball, 8 x 9)
-	B5	VFPGA (90-ball, 8 x 13)
-	CF	VFPGA (60-ball, 8 x 10)
-	CK	VFPGA (60-ball, 10 x 11.5)
-	CM	VFPGA (90-ball, 10 x 13)
-	CX	VFPGA (90-ball, 9 x 13)
-	JG	PoP (168-ball, 12 x 12)
<b>Mobile LPSDR</b>		
-	B4	VFPGA (54-ball, 8 x 8)
-	B5	VFPGA (90-ball, 8 x 13)
-	BF	VFPGA (54-ball, 8 x 9)
-	CJ	VFPGA (54-ball, 10 x 11.5)
-	CM	VFPGA (90-ball, 10 x 13)

\*Due to space limitations, FBGA- and µBGA-packaged components and flip chips in packages have an abbreviated part mark that is different from the part number. See our Web site for more information on abbreviated component marks.  
 \*\*\*Dimensions in millimeters  
 Some device offerings are available in a VFPGA rather than an FBGA package; this is noted on the data sheet.

© 2012 Micron Technology, Inc.  
 Micron and the Micron Logo are trademarks of Micron Technology, Inc. RLD RAM is a registered trademark of Qimonda AG in various countries, and is used by Micron Technology, Inc. under license from Qimonda. Products and specifications are subject to change without notice. Dates are estimates only.

