DDR3 RDIMMs Channel

Basics, Topology, Simulations, and Timing

4/12/2007

Agenda

- DDR3 RDIMM Basics and Introduction
- DDR3 RDIMM – Topology, Simulation, and Timing
  - General System Assumptions
  - Improved Topology
  - Address/Command/Control
  - Clock
  - Data
- DDR3 RDIMM – Raw Cards and Types
- DDR3 RDIMM – Early Development and Micron Support

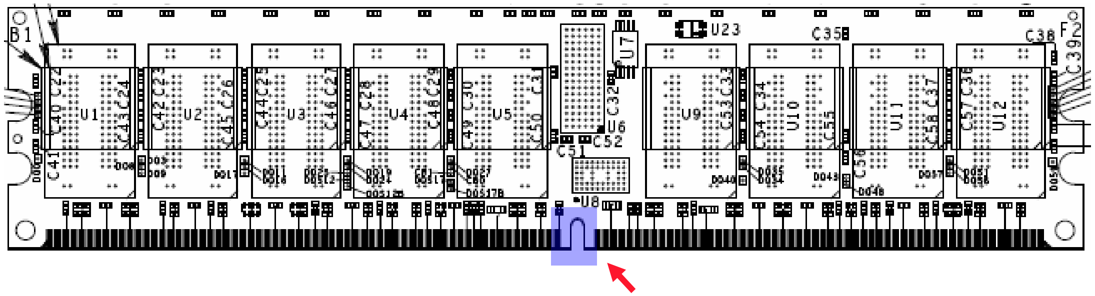
DDR3 RDIMM

Basics and Introduction

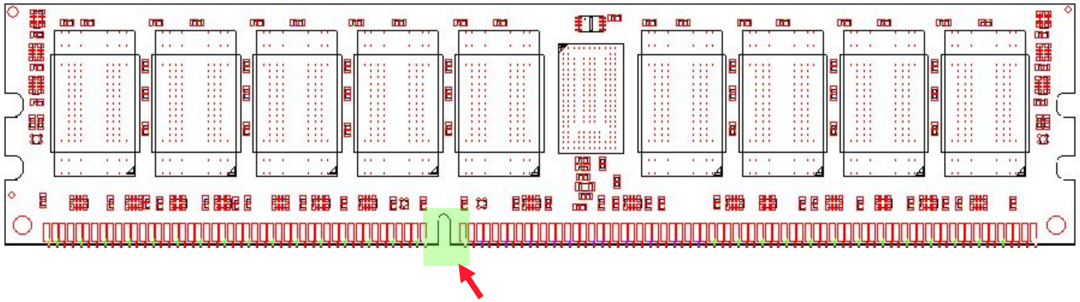
4/12/2007

Form Factor

- The DDR3 RDIMMs keep the same 240-pin edge connector as DDR2 RDIMMs, but with a different key placement



For DDR2 the key is between pins 64/65



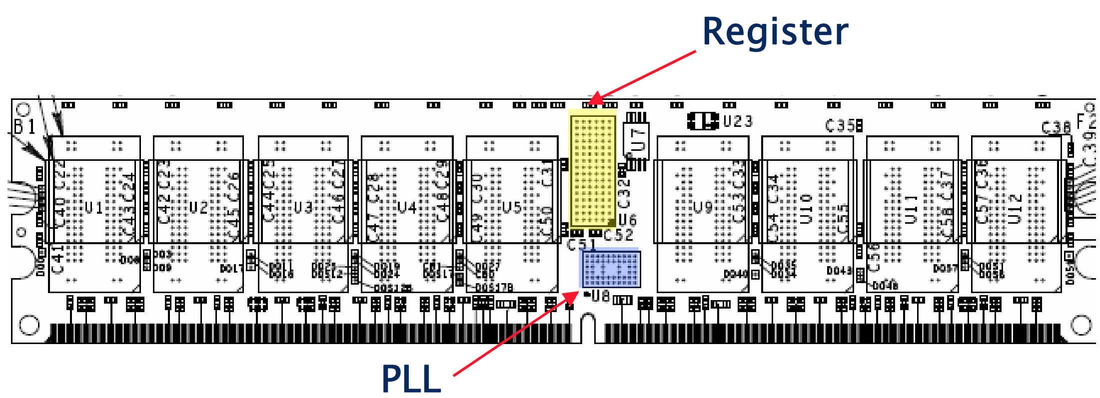
For DDR3 the key is located between pins 48/49

Note the DDR3 RDIMM and DDR3 UDIMM utilize the same edge connector

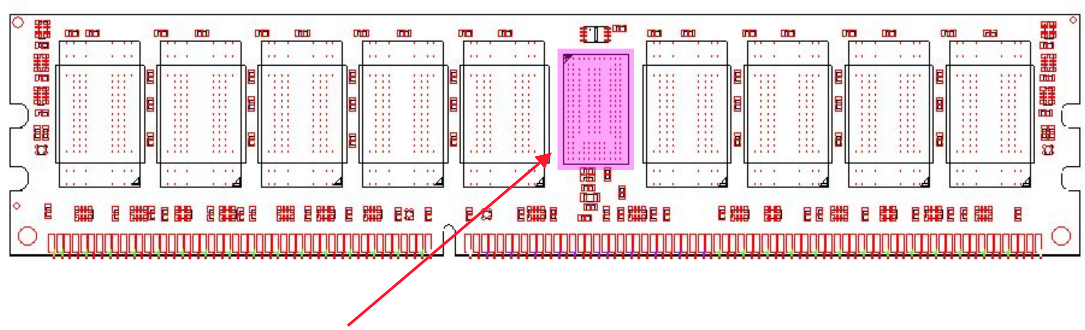
Logic/Drivers

- The DDR3 RDIMMS look a bit different as the PLL is now included in the same package as the register

DDR2 RDIMM >>>



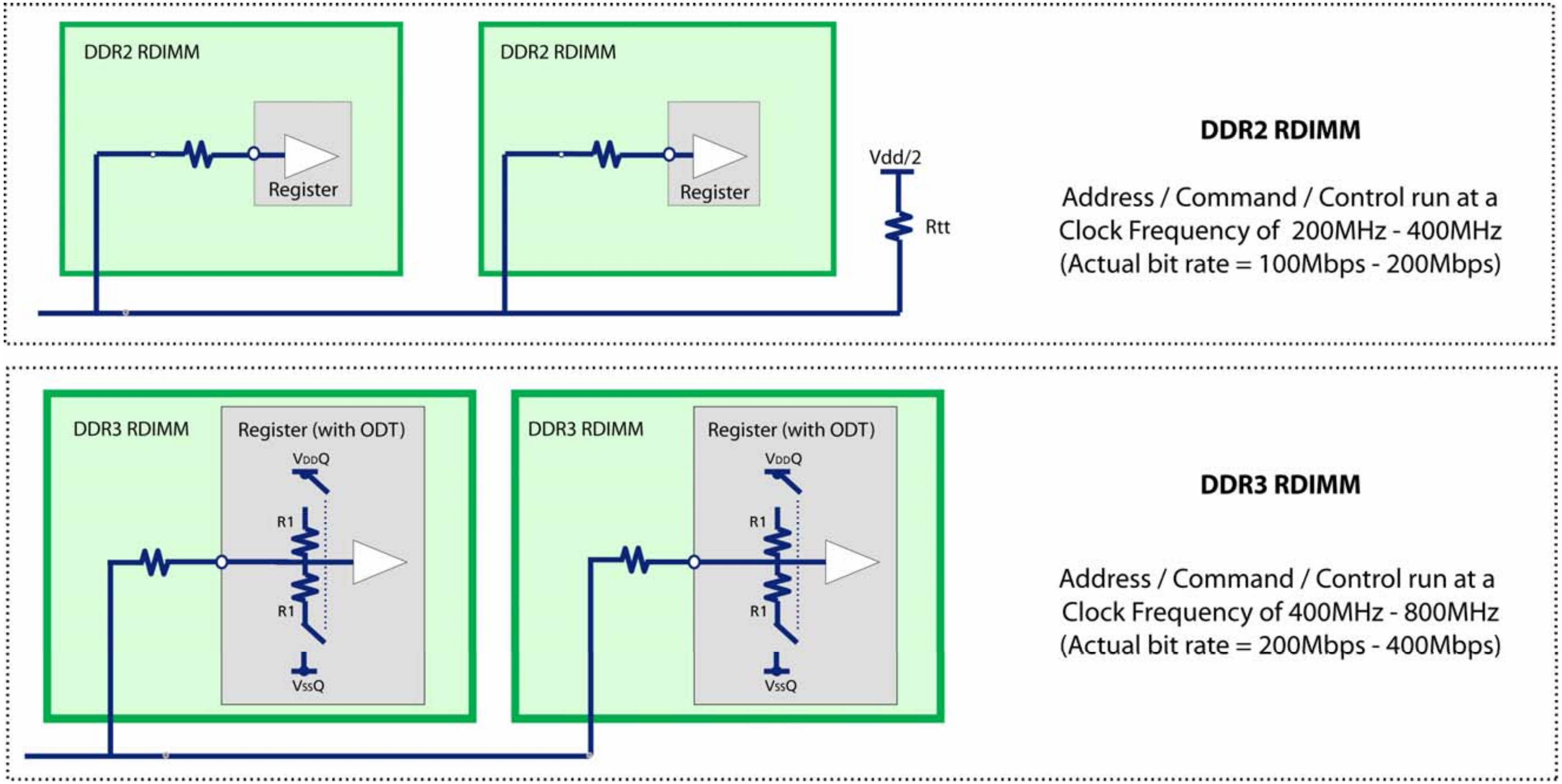
DDR3 RDIMM >>>



PLL and register are combined into a single package

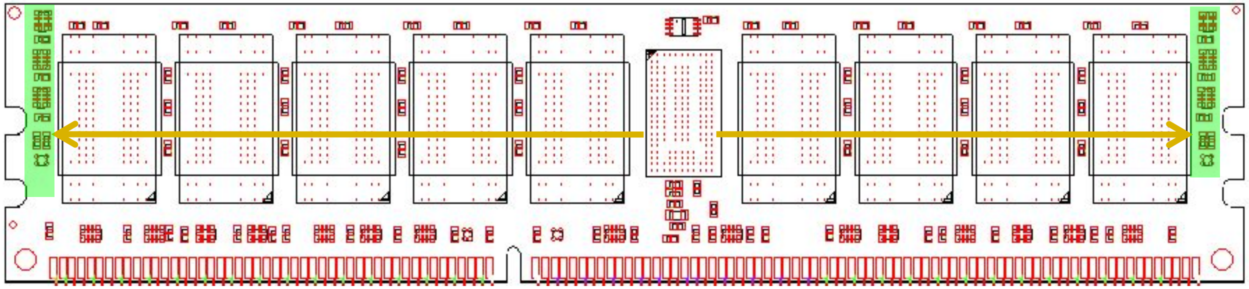
Improved Termination for Pre-Register

- New for DDR3 – the address / command registers utilize optional On-Die-Termination (ODT)



Improved Termination for Post-Register

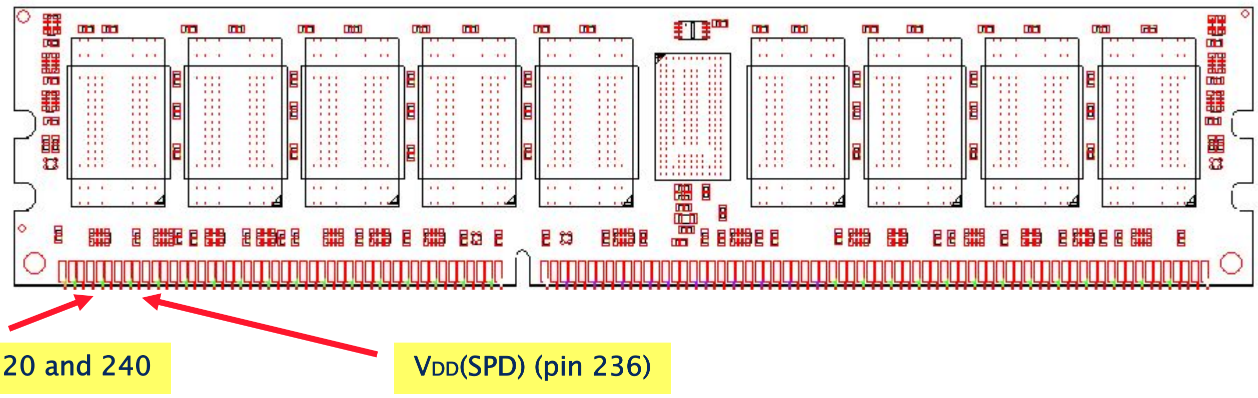
- Due to the "Flyby" layout:
  - The clock/address/command/control traces feed both sides of the module in a fly-by method
    - To better balance Vtt power, most (Left/Right side) address signals are inverted
    - This signal group arrive at the DRAM simultaneously, but there is a flight time variation between the different DRAM locations



    - Termination resistors have been added to the module and are placed at both ends of the module

Additional Power Pins

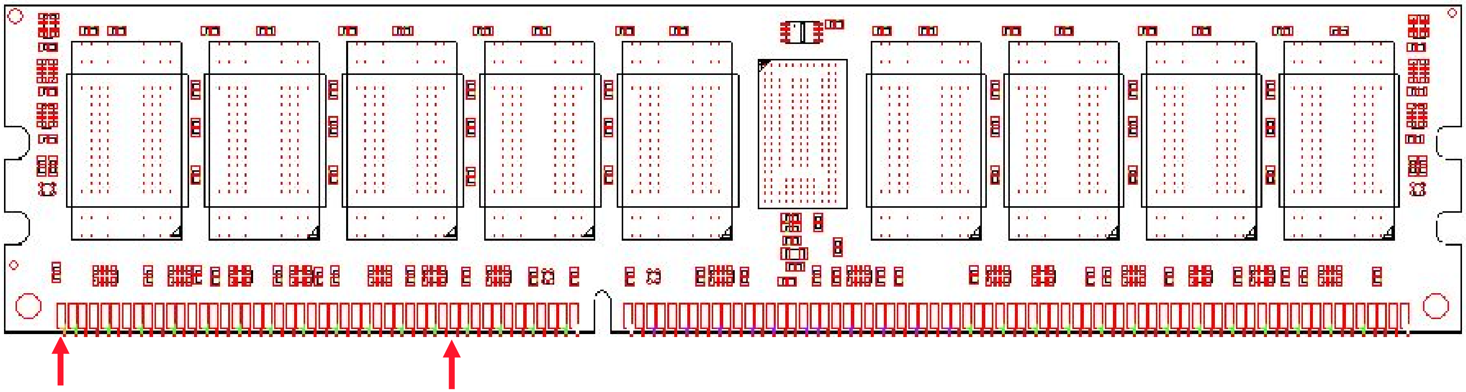
- DDR3 RDIMMs now require Vtt power
  - Vtt power edge connector pins at 48, 49, 120 and 240



- To accommodate the temperature sensor option VDD(SPD), the voltage requirements for the EPROM has changed
  - For DDR2 VDD(SPD) was 1.8V – 3.6V
  - For DDR3 VDD(SPD) is 3.0V – 3.6V

New Voltage Pins and Levels

- DRAM core and I/O voltage levels, V_{DD}/V_{DDQ} = 1.5V
- To help improve address/command voltage margins DDR3 RDIMMs also have isolated Vref, routed on two different (wide) traces
    - V_{REF}(DQ) is for data
    - V_{REF}(CA) is for command/address



Data Channel – Loads

- The DDR3 data channel is much like the DDR2 channel, although DDR3 data rates are twice as fast
  - DDR3 data rates range from 800MT/s to 1,333MT/s and with plans to support up to 1.6GT/s
- Most systems will support a maximum of two slots per channel up to 1,066MT/s (or 4 data loads)

	Number of RDIMMS	* DQ Loads
DDR3-800	Two - (DR)	4
DDR3-1067	Two - (DR)	4
DDR3-1333	Two - (DR)	Target (4)

** early assumptions*

Improvements to the Data Channel

- The DDR3 data channel can run faster due to enhancements in the DDR3 component
  - DDR3 supports dynamic ODT
    - Dynamic ODT allows the termination value to change without issuing an MRS command, which essentially changes the ODT termination "on-the-fly"
    - With Dynamic ODT enabled, the DRAM will switch from {normal} ODT to Dynamic ODT (RTT_WR) when beginning a write burst; and will subsequently switch back to ODT (RTT_nom) at the completion of the write burst
  - DDR2 ODT values reflect only: 50Ω, 75Ω, 150Ω
  - DDR3 ODT values include: 20Ω, 30Ω, 40Ω, 60Ω, 120Ω

Optional Temperature Sensor

- Optional Temperature Sensor
  - Temperature reporting and threshold settings are accessed through the SMBus
  - Threshold crossing is indicated on RDIMM pin 187 using an open drain output
  - 12 bit resolution
    - Has +/- 2°C accuracy, but could be better in the future
  - -20°C to +125°C range
  - Supply voltage 3.0V to 3.6V (same as EEPROM V_{DD}(SPD))
- Early temperature sensor data sheets available

Agenda

- DDR3 RDIMM Basics and Introduction
- DDR3 RDIMM – Topology, Simulation, and Timing
  - General System Assumptions
  - Improved Topology
  - Address/Command/Control
  - Clock
  - Data
- DDR3 RDIMM – Raw Cards and Types
- DDR3 RDIMM – Early Development and Micron Support

DDR3 RDIMM
Topology, Simulation, and Timing

General System Assumptions

4/12/2007

General System Assumptions

- Although your actual values may vary, Micron has used the following preliminary system level assumptions in our simulations
- These should be referenced for a design starting point only
  - A complete system simulation and timing analyses must be completed to ensure functionality

General System Assumptions

- System Board Lead-in Nominal Impedance (UDIMM)

System Board Lead-in Nominal Impedance and Reference		
DQ	40-ohms to 50-ohms	Ground
DQS/DQS (SINGLE ENDED)	40-ohms to 50-ohms	Ground
CMD/Address	40-ohms to 50-ohms	Ground
Control	40-ohms to 50-ohms	Power
Clocks (Differential)	40-ohms to 50-ohms	Power

  - For least amount of noise, all lead-In traces should be “strip-line”
  - Signals should be power or ground plan reference

General System Assumptions

- Controller Break out Impedance and lengths used for initial simulations (UDIMM)

Controller Break out Impedance		Length range for breakout
DQ	50-ohms to 60-ohms	0.2" to 1.0"
DQS/DQS (SINGLE ENDED)	50-ohms to 60-ohms	0.2" to 1.0"
CMD/Address	50-ohms to 60-ohms	0.2" to 1.0"
Control	50-ohms to 60-ohms	0.2" to 1.0"
Clocks	50-ohms to 60-ohms	0.2" to 1.0"

General System Assumptions

- System Board Lead-in Length (inches) including breakout (UDIMM)

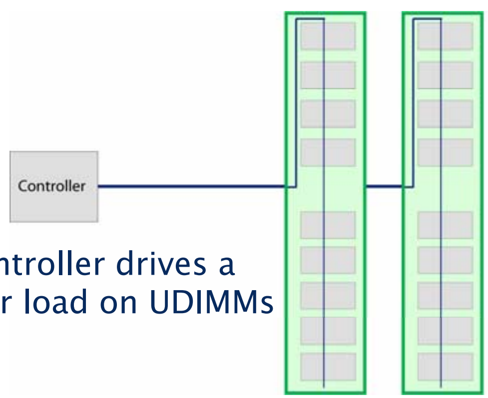
System Board Lead-in Length (inches) including breakout	
DQ/DQS	1.0" to 7.0"
CMD/Address	1.0" to 5.0"
Control	1.0" to 5.0"
Clocks	1.0" to 5.5"

  - Byte lane lengths do not need to match, but within each byte lane the lengths and propagation delay should match

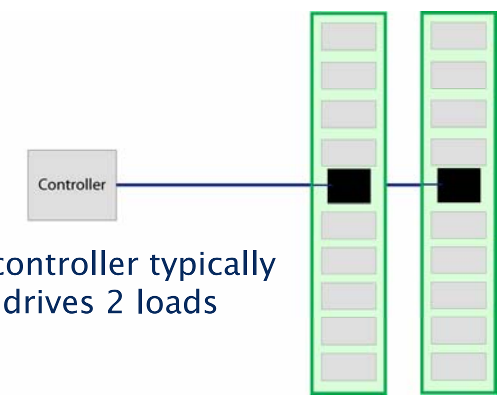
General System Assumptions

- Ron Nominal Drive strength in ohms (UDIMM)
  - Actual register values from different vendors may vary

Ron Nominal Drive strength in Ohms	
DQ	30-ohms to 40-ohms (1& 2-slots/ch)
Control	30-ohms to 40-ohms (1 & 2-slots/ch)
C/A	20-ohms to 40-ohms (2-slots/ch) 30-ohms to 40-ohms (1-slot/ch)
Clock	30-ohms to 40-ohms (1 & 2-slots/ch)



Controller drives a heaver load on UDIMMs



RDIMM controller typically only drives 2 loads

General System Assumptions

- Driver slew rate (Controller) – UDIMM

Driver slew rate (Controller)		
DQ V/ns	2V/ns to 5V/ns (PVT range)	into 50-ohms test load pulled up to VddQ/2
Control V/ns	1V/ns to 3V/ns (PVT range)	into 50-ohms test load pulled up to VddQ/2
CMD/Address V/ns	1V/ns to 3V/ns (PVT range)	into 50-ohms test load pulled up to VddQ/2
Clock V/ns	2V/ns to 5V/ns (PVT range)	into 50-ohms test load pulled up to VddQ/2

General System Assumptions

- Typical RDIMM spacing (UDIMM)

Typical RDIMM spacing	
Distance between RDIMMs in a 2-slots/ch system	0.4" to 0.6"

  - Note: additional DIMM spacing may be required for module thermal aspects

DDR3 RDIMM
Topology, Simulation, and Timing

Improved Topology, Fly-by

4/12/2007

Micron

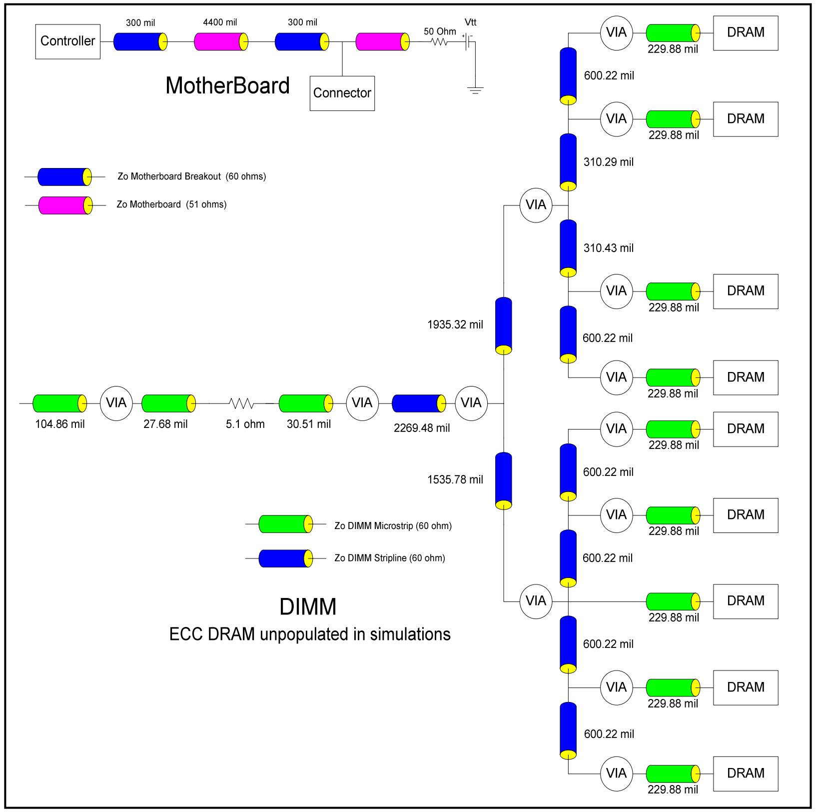
Comparison of Tree to Fly-By

- DDR2 clock/command/control and addresses use a "tree" topology
  - Each branch has multiple loads and stubs
  - V_{TT} termination is on the system board and not at the end of the individual stubs
- DDR3 uses a "fly-by" topology
  - The stub to each individual DRAM is very short
  - There is V_{TT} termination at the far end of the bus

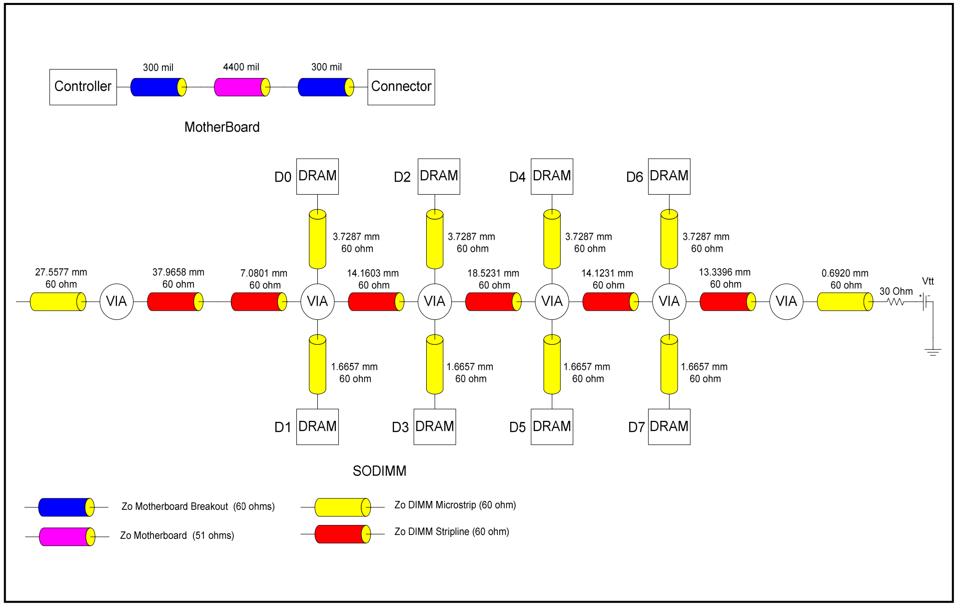
Comparison of Tree to Fly-By

- An example comparing the address structure of the two topologies

Tree Topology (SR x8 w/ECC)



Fly-By Topology (SR x8)

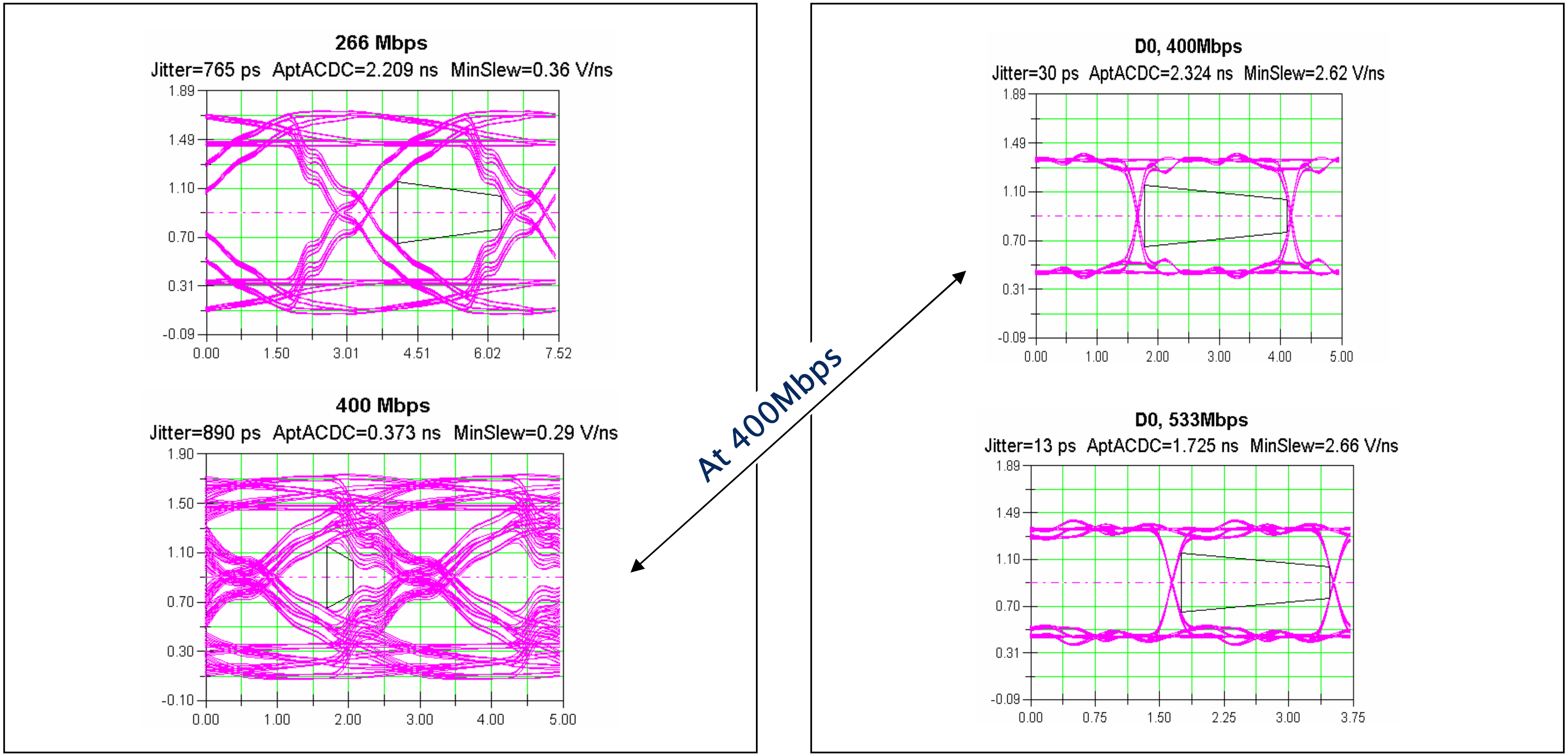


Comparison of Tree to Fly-By

- Address data eye diagrams at the DRAM (1T)

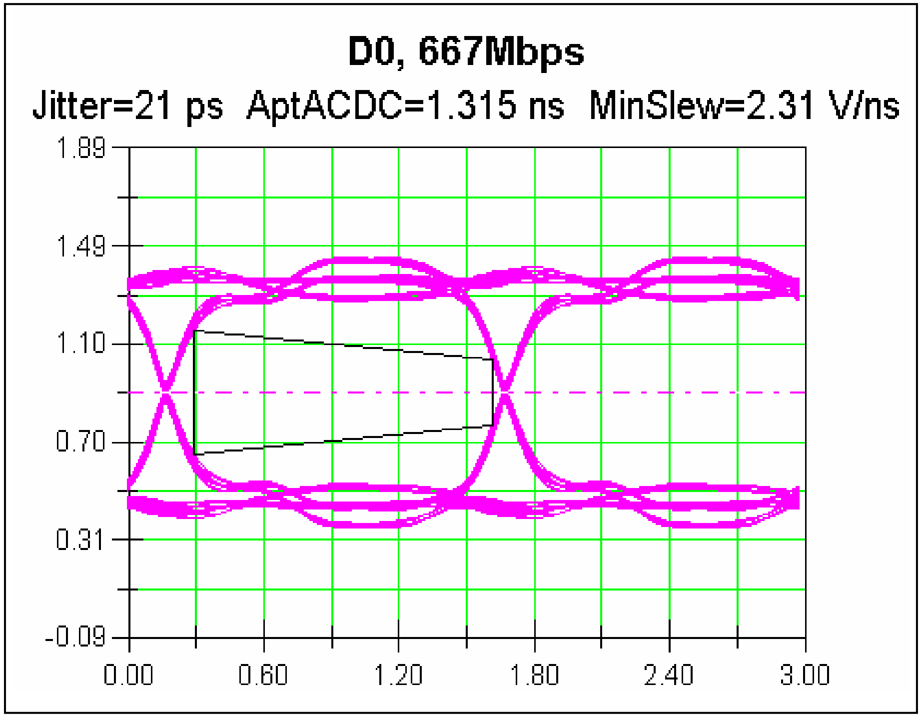
Tree Topology

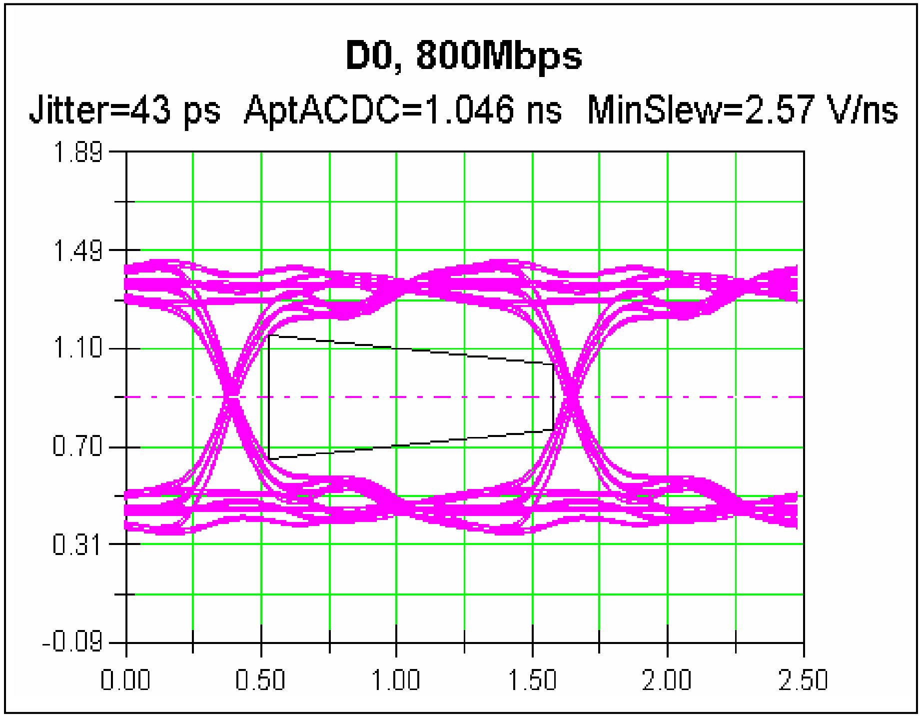
Fly-By Topology



Comparison of Tree to Fly-By

- For DDR3, the address/command and control are designed to operate up to 800Mbps (DDR3-1600)



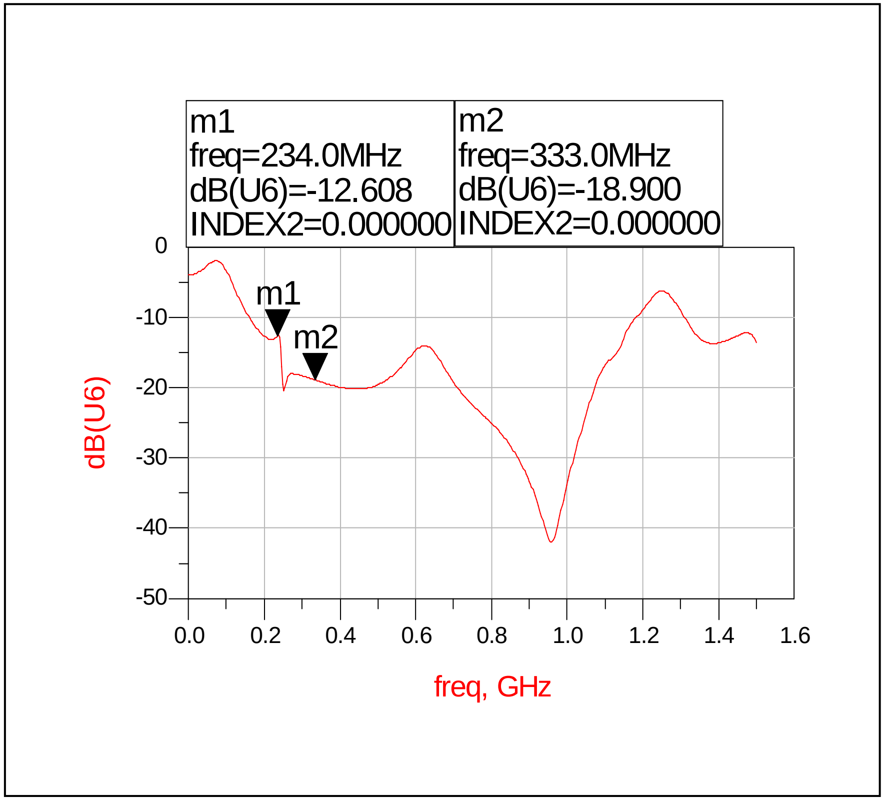


Fly-By Topology (Only)

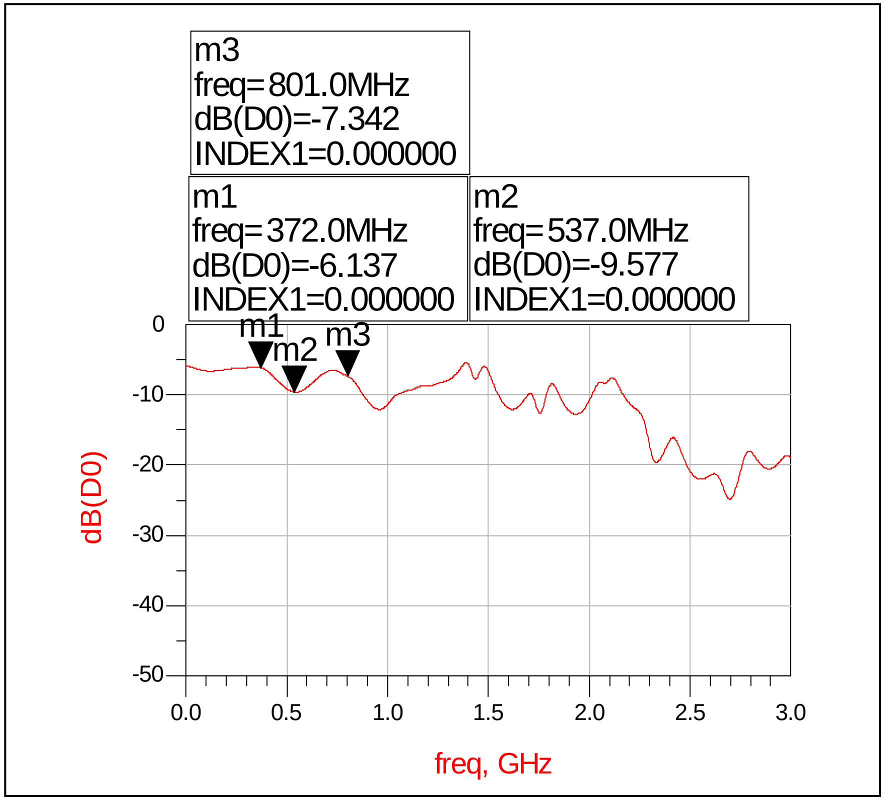
Comparison of Tree to Fly-By

- Typical frequency response for:

Tree Topology



Fly-By Topology



Comparison of Tree to Fly-By

Tree Bus Topology

- Pros
  - Arrival time skew at various DRAM devices could be made very small (negligible)
- Cons
  - Less data-eye margin

Fly-By Topology

- Pros
  - High bandwidth
  - It could be terminated better than tree bus at far end of the bus
- Cons
  - Arrival time skew at various DRAM devices

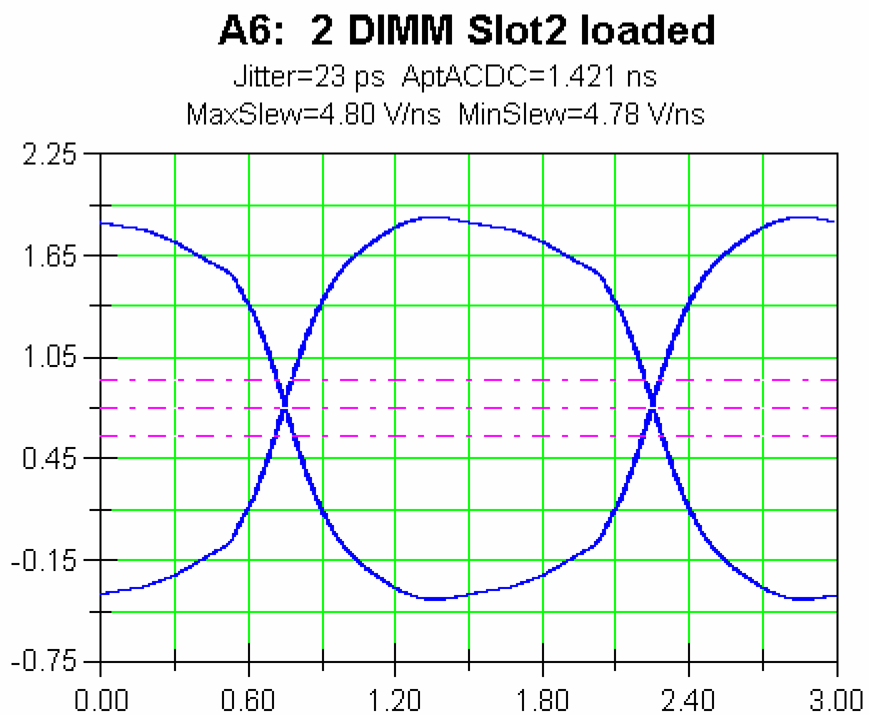
DDR3 RDIMM
Topology, Simulation, and Timing

Command Bus and Timing
(Pre-Register and Post-Register)

4/12/2007

Pre Register Address Timing Example (Light Load)

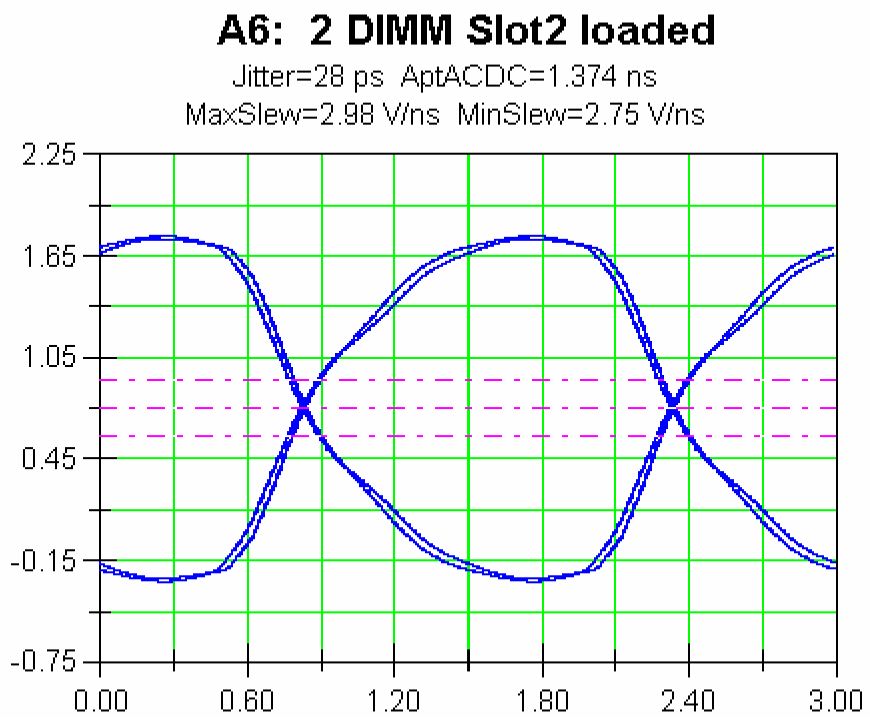
- Pre-Register Timing DDR3-1333 (clock rate = 667 MHz)
  - Single R/C A (SRx8) module, in system
  - Measured at Slot 2



*The PRBS pattern will have a slightly smaller aperture

Pre Register Address Timing Example (Light Load)

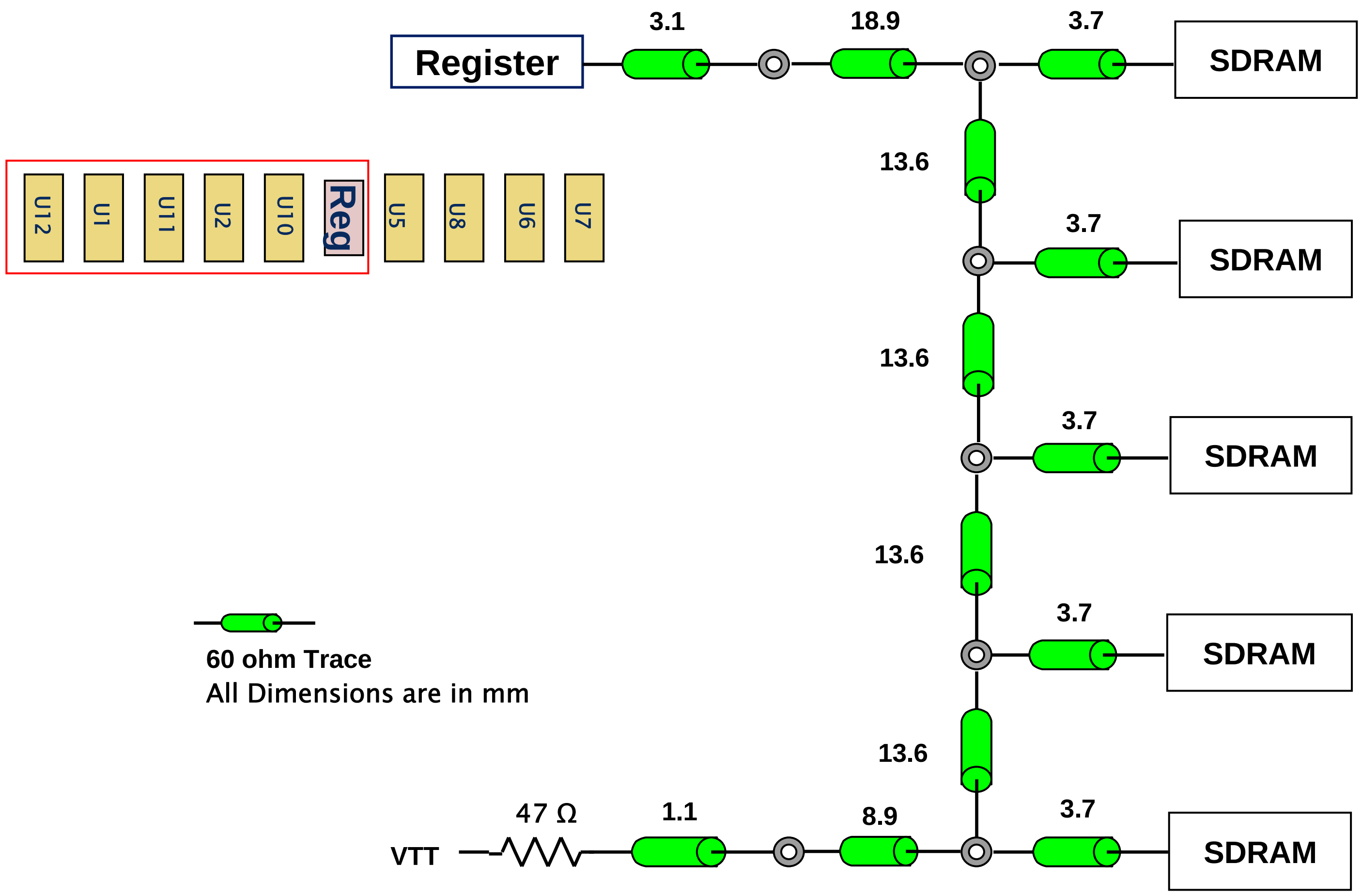
- Pre-Register Timing DDR3-1333 (clock rate = 667 MHz)
  - Two R/C A (SRx8) modules, in system
  - Measured at Slot 2



*The PRBS pattern will have a slightly smaller aperture

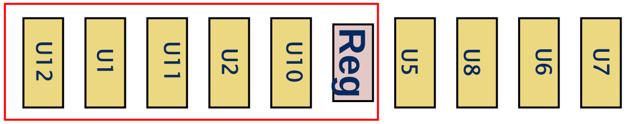
Post Register Address Timing Example (Light Load)

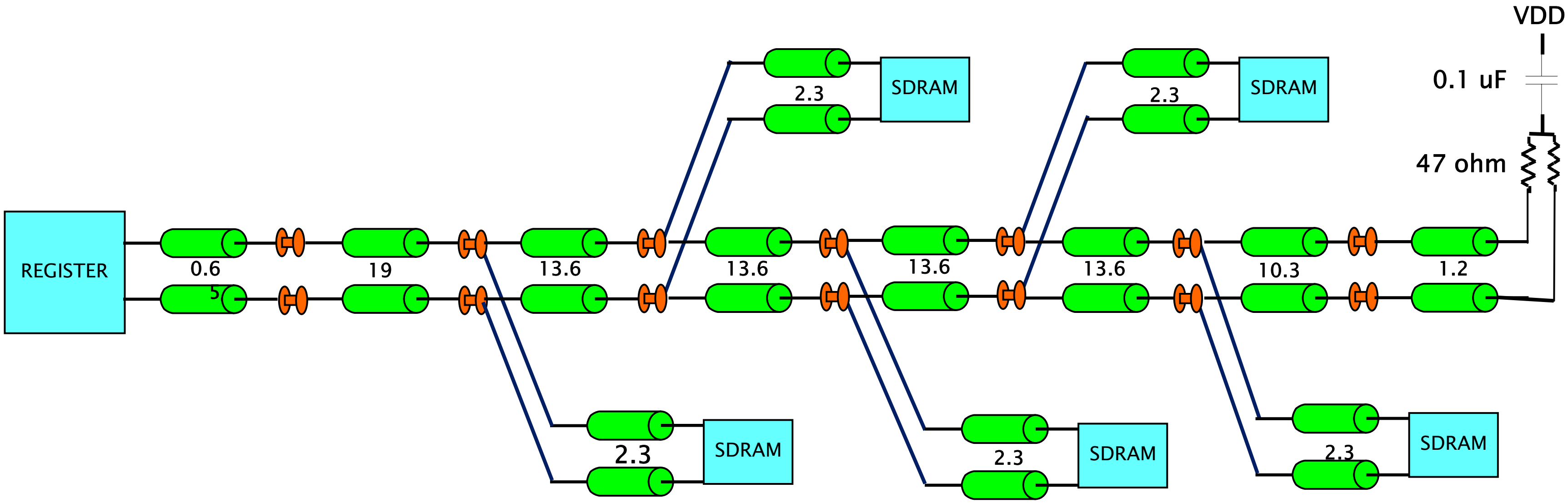
- Topology for address/command/control left side

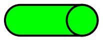


Post Register Address Timing Example (Light Load)

- Topology for clock left side





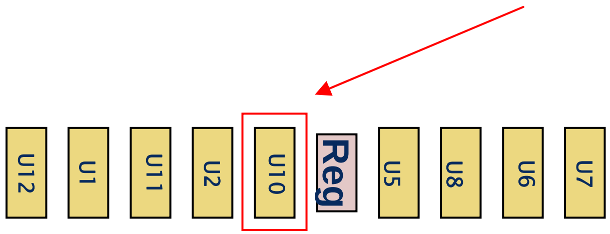


60 ohm Trace

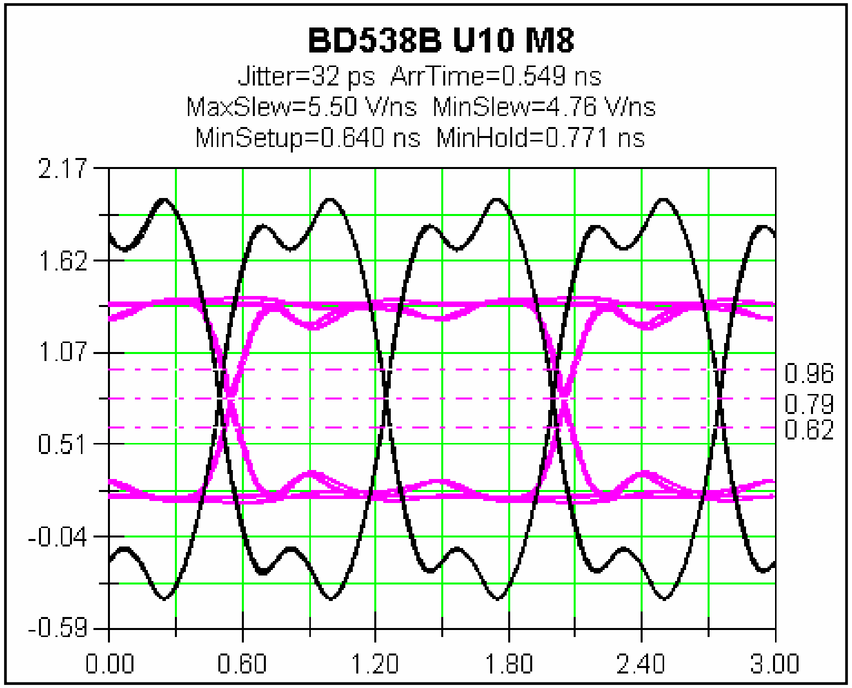
All dimensions are in mm

Post Register Address Timing Example (Light Load)

- POST-Register Timing Address to Clock
  - DDR3-1333 (clock rate = 667.67 MHz)
  - Single R/C A (SRx8) module in system
  - Measured at first DRAM to the left of the register

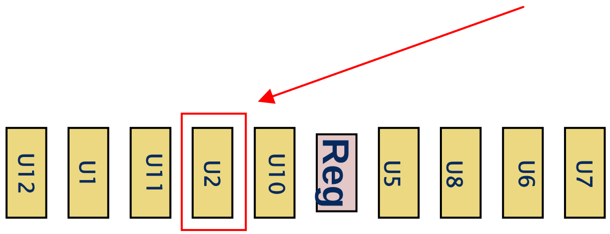


- Using a moderate driver 20-25 ohms
- Fast Corner
- Clock shown as single ended
- DRAM tIS = 225ps tIH = 225ps

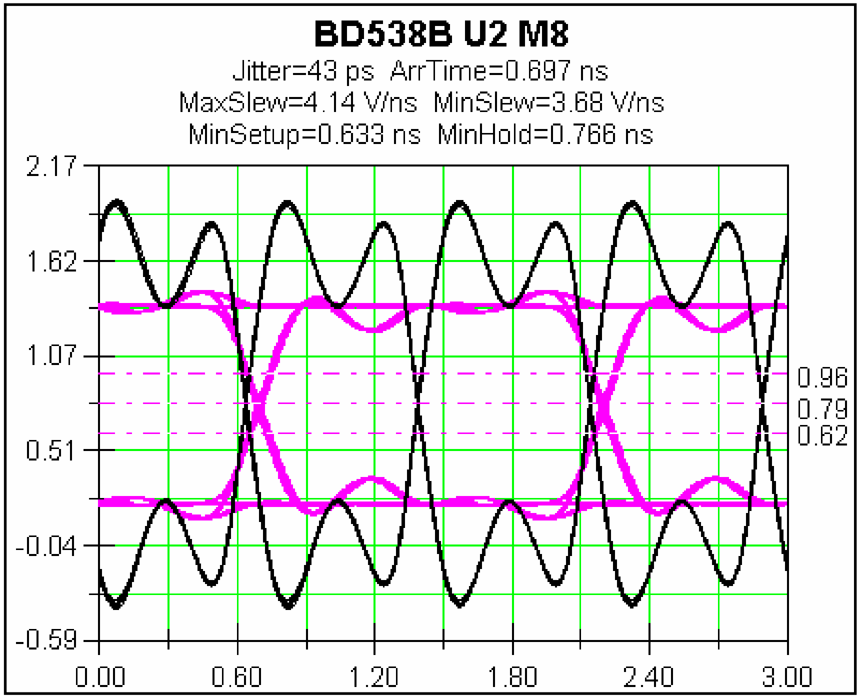


Post Register Address Timing Example (Light Load)

- POST-Register Timing Address to Clock
  - DDR3-1333 (clock rate = 667.67 MHz)
  - Single R/C A (SRx8) module in system
  - Measured at second DRAM to the left of the register

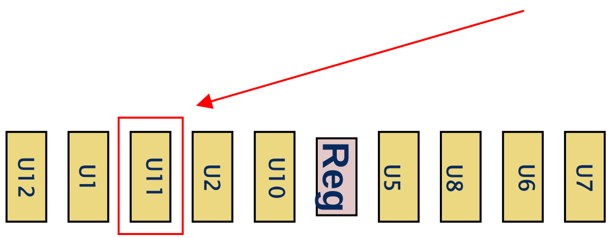


- Using a moderate driver 20-25 ohms
- Fast Corner
- Clock shown as single ended
- DRAM tIS = 225ps tIH = 225ps

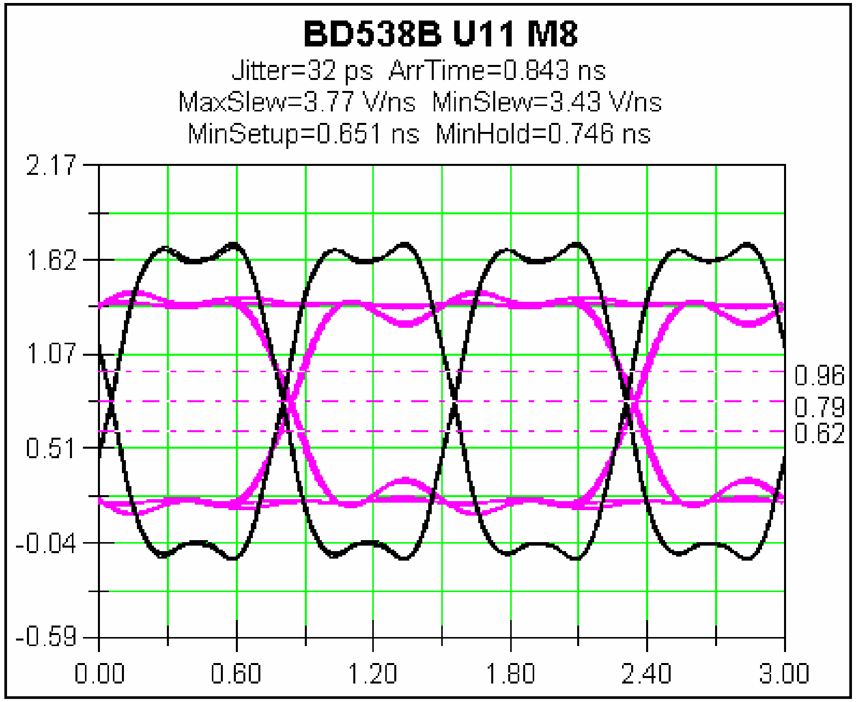


Post Register Address Timing Example (Light Load)

- POST-Register Timing Address to Clock
  - DDR3-1333 (clock rate = 667.67 MHz)
  - Single R/C A (SRx8) module in system
  - Measured at third DRAM to the left of the register

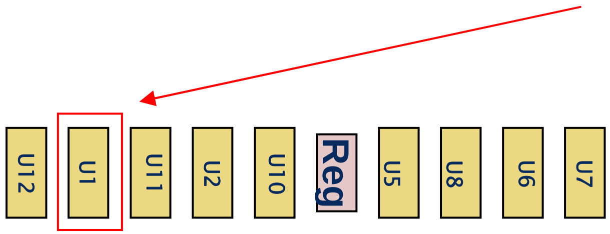


- Using a moderate driver 20-25 ohms
- Fast Corner
- Clock shown as single ended
- DRAM tIS = 225ps tIH = 225ps

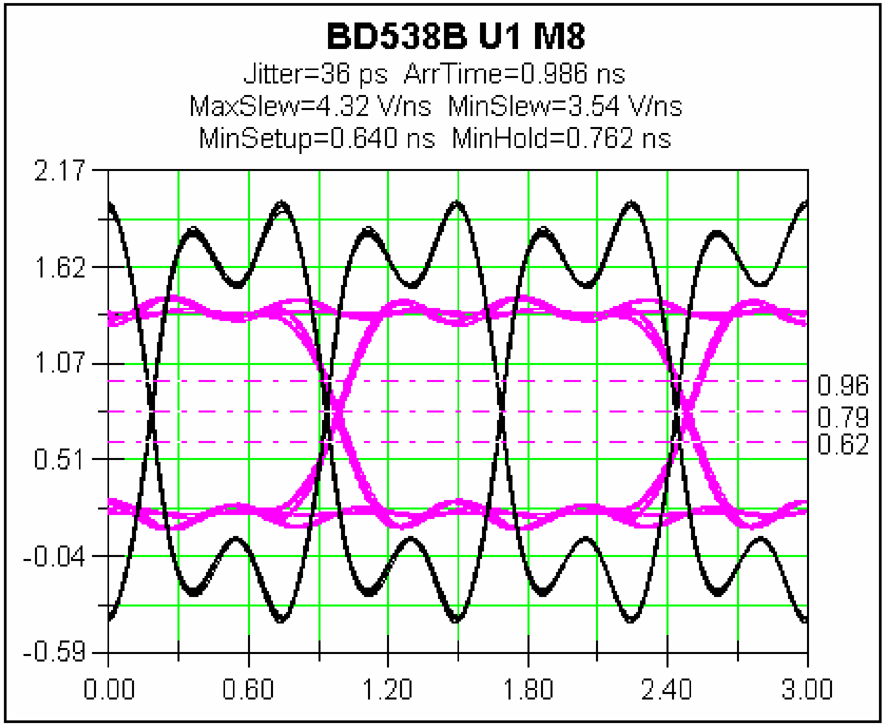


Post Register Address Timing Example (Light Load)

- POST-Register Timing Address to Clock
  - DDR3-1333 (clock rate = 667.67 MHz)
  - Single R/C A (SRx8) module in system
  - Measured at forth DRAM to the left of the register

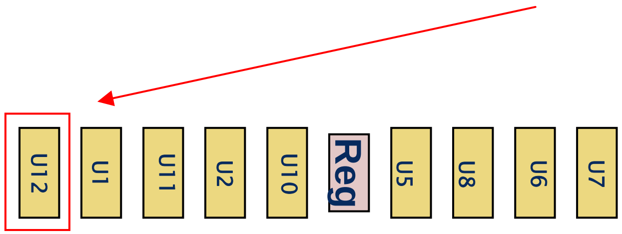


- Using a moderate driver 20-25 ohms
- Fast Corner
- Clock shown as single ended
- DRAM tIS = 225ps tIH = 225ps

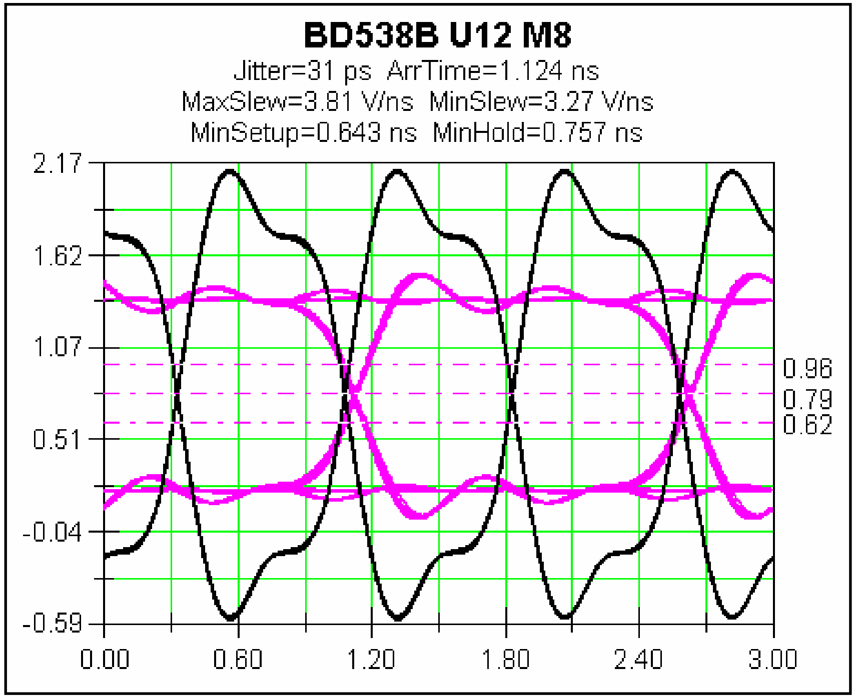


Post Register Address Timing Example (Light Load)

- POST-Register Timing Address to Clock
  - DDR3-1333 (clock rate = 667.67 MHz)
  - Single R/C A (SRx8) module in system
  - Measured at fifth DRAM to the left of the register

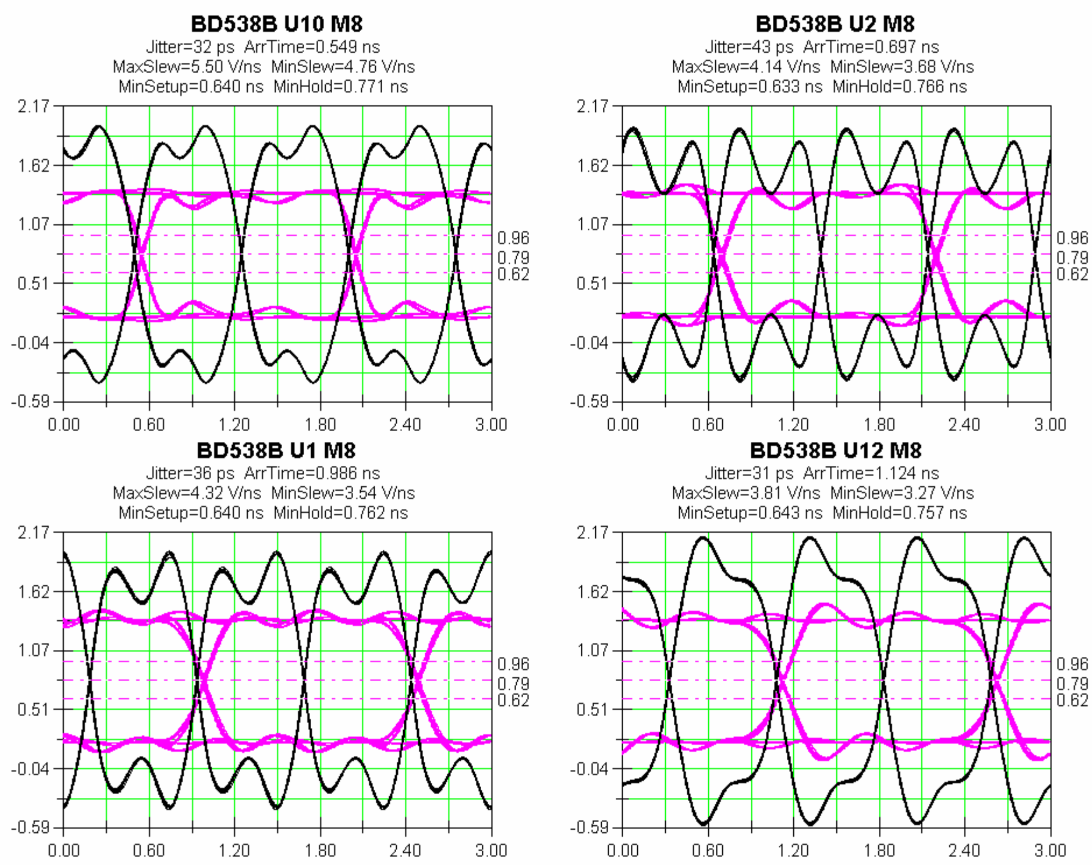


- Using a moderate driver 20-25 ohms
- Fast Corner
- Clock shown as single ended
- DRAM tIS = 225ps tIH = 225ps



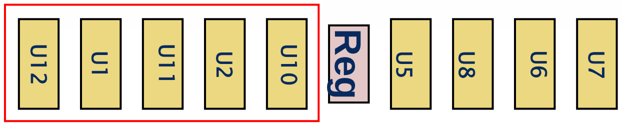
Post Register Address Timing Example (Light Load) – SR x8

- Fast Corner @ 1,333MT/s (clock = 667 MHz)



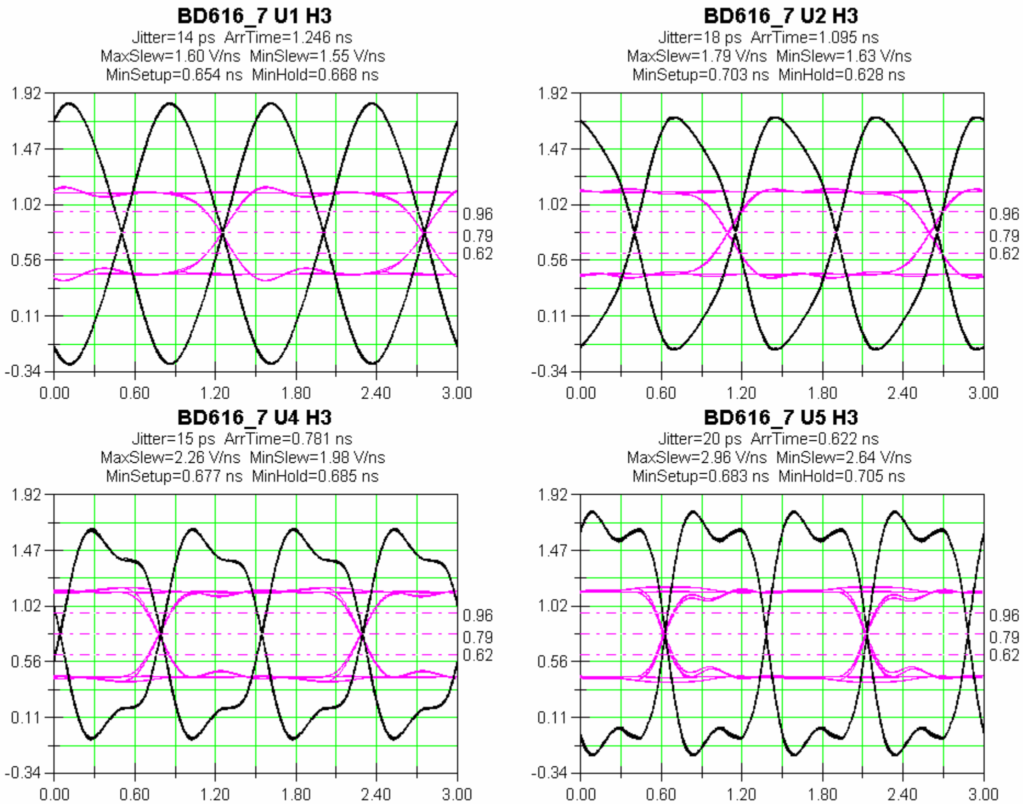
POST-Register Timing Clock

- Single R/C A (SRx8) module in system
- DDR3-1333 (clock rate = 667 MHz)
- Shows all CK0A and A6A from the left side

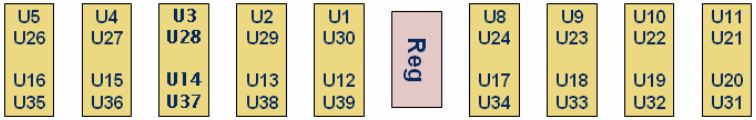


Post Register Address Timing Example (Heavy Load) – DR x4

- Fast Corner @ 1,333MT/s (clock = 667 MHz)



R/C J , DR x4 (36 DRAM)
Shown with differential clocks
<u>CK0A</u> with moderate drive
<u>WEA</u> with moderate drive



DDR3 RDIMM
Topology, Simulation, and Timing

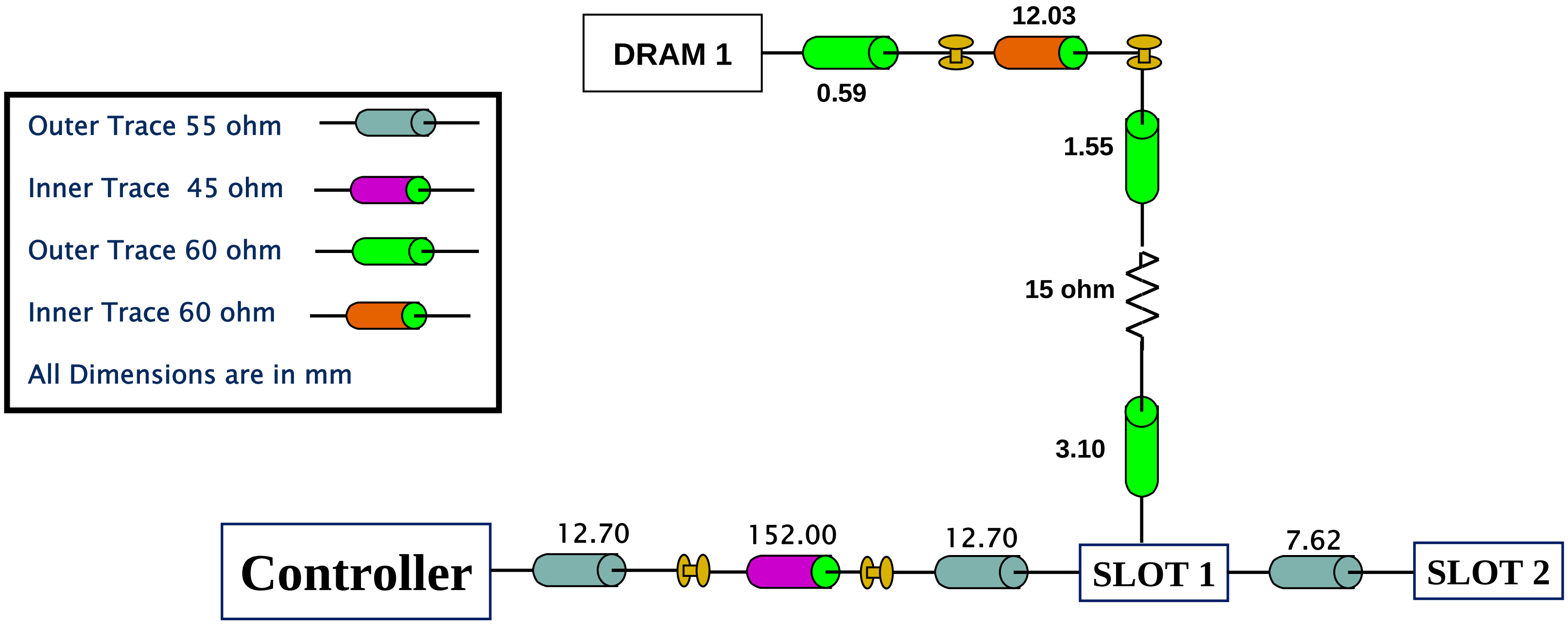
Data Bus and Timing

4/12/2007

Micron

Data Bus

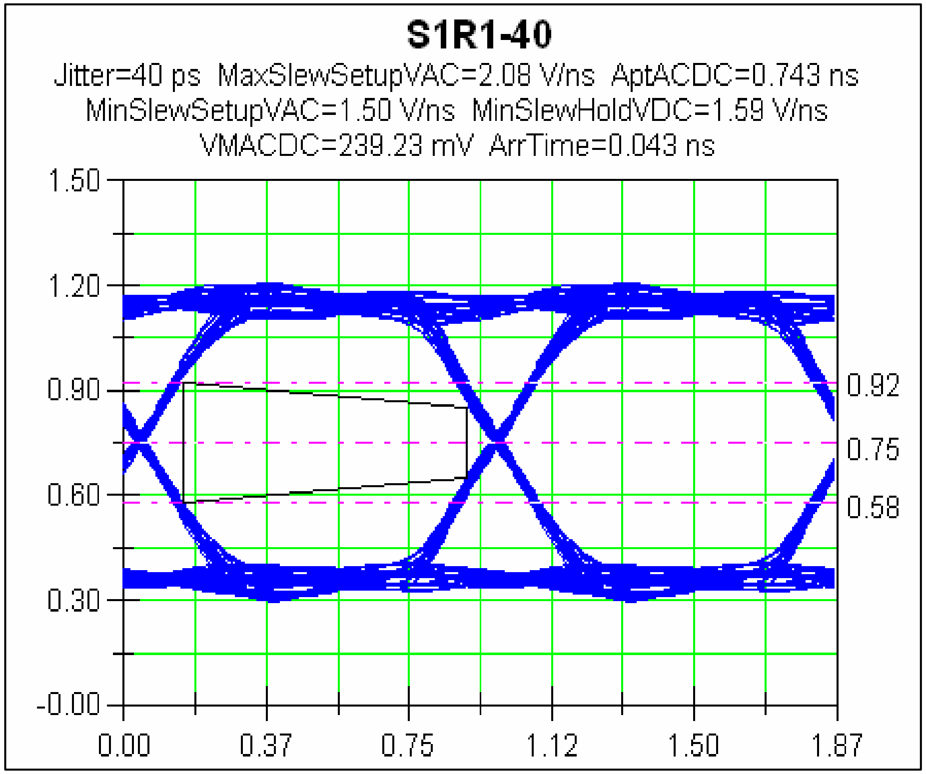
- Topology (single slot) DR x4



Data Bus

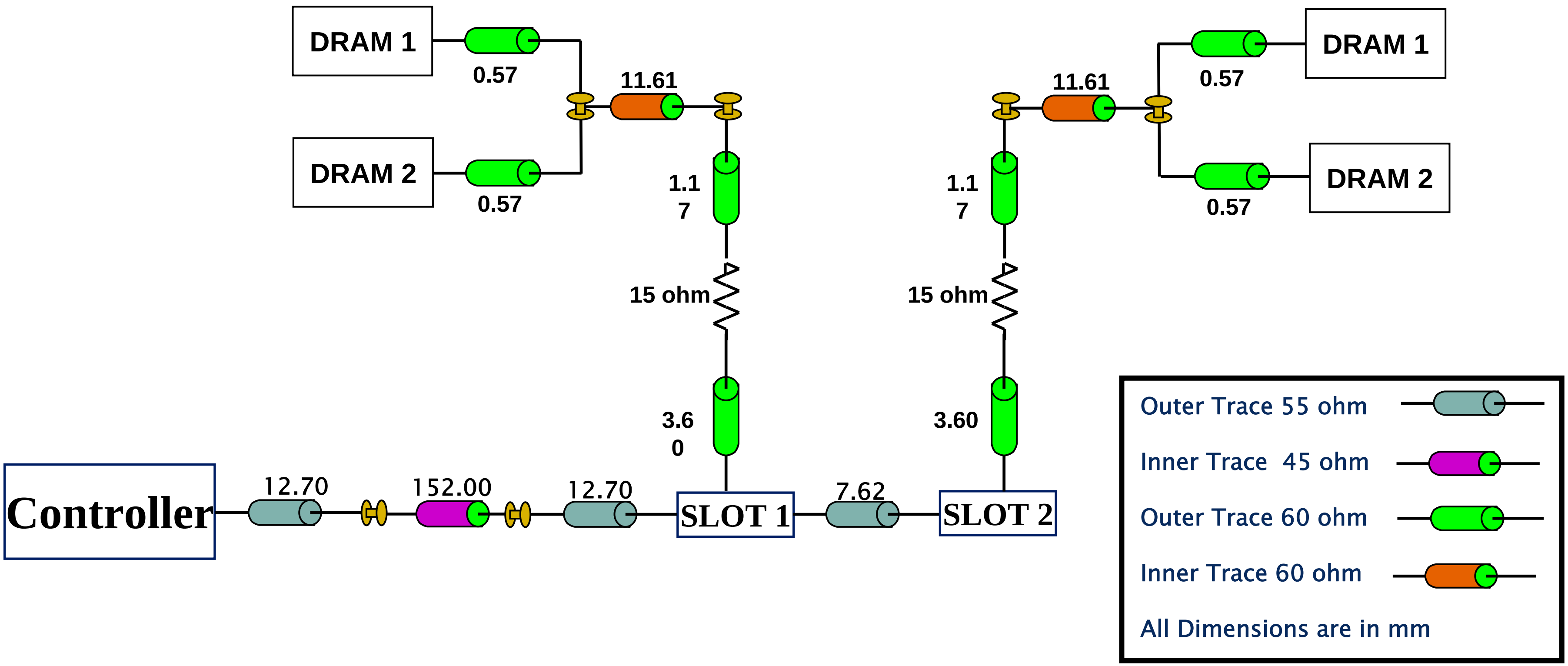
- Single slot populated (DR x4)
- Write to Slot 1, Rank 1
- Signal probed at DRAM

Clock Rate = 533 MHz (DDR3-1066)



Data Bus

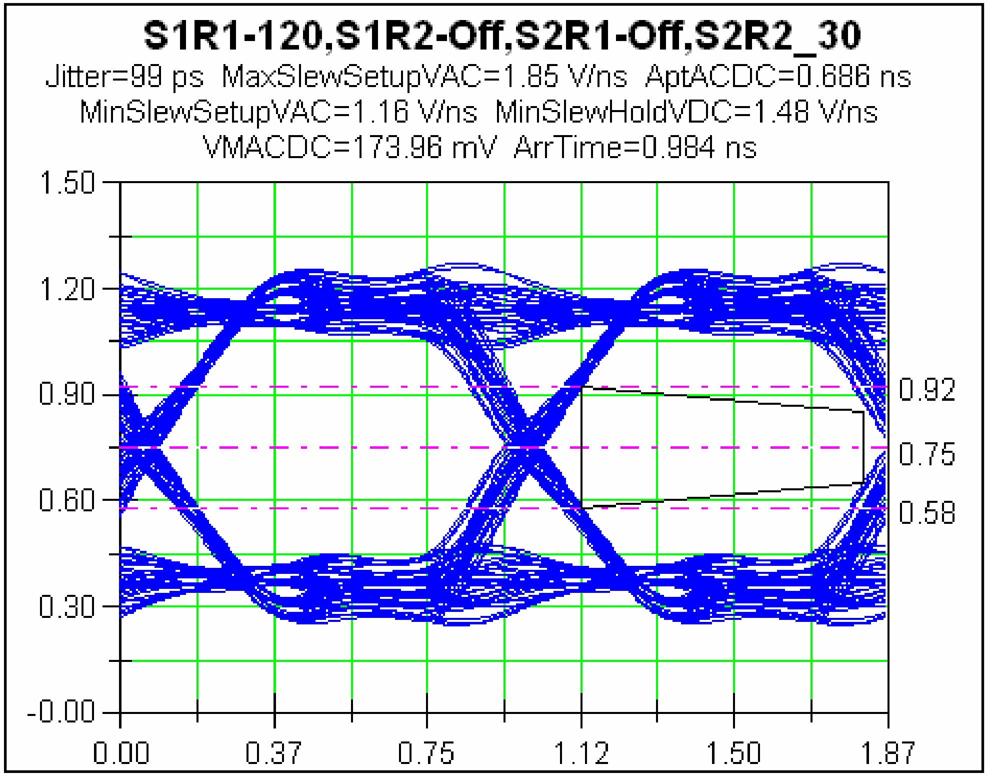
- Topology (both slots) DR x4



Data Bus

- Both slots populated (DR x4)
- Write to Slot 1, Rank 1
- Signal probed at DRAM

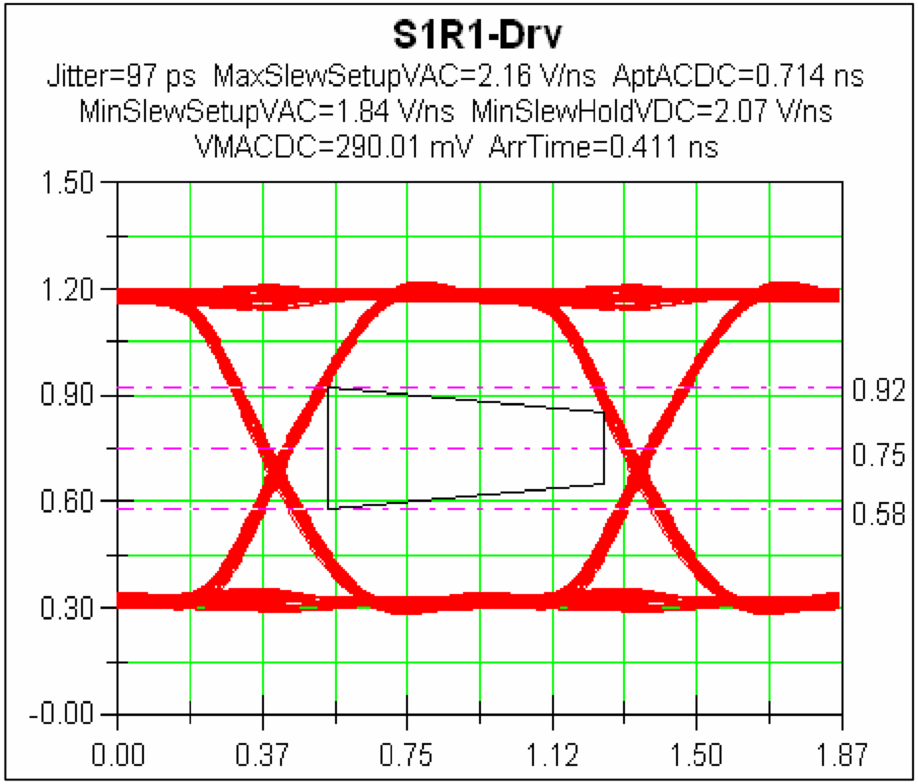
Clock Rate = 533 MHz (DDR3-1066)



Data Bus

- Single slot populated (DR x4)
- READ from Slot 1, Rank 1
- Signal probed at Controller, Controller ODT = 75 ohm

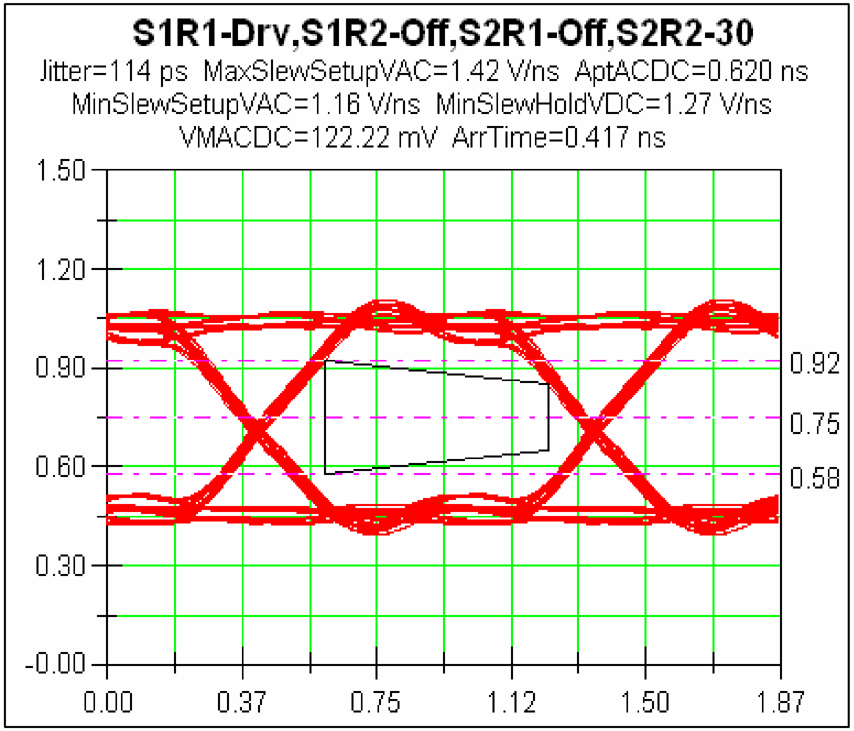
Clock Rate = 533 MHz
(DDR3-1066)



Data Bus

- Both slots populated (DR x4)
- READ from Slot 1, Rank 1
- Signal probed at Controller, Controller ODT = 75 ohm

Clock Rate = 533 MHz
(DDR3-1066)



DRAM On-Die-Termination (ODT) Suggestions

- WRITE Table for a two slot channel
  - For transfer rates of 1,066Mb/s

		Write To	Controller ODT	Slot 1		Slot 2	
Slot 1	Slot 2			Rank 1	Rank 2	Rank 1	Rank 2
DR	DR	Slot 1	off	120Ω	ODT off	ODT off	30Ω
		Slot 2	off	ODT off	30Ω	120Ω	ODT off
DR	SR	Slot 1	off	120Ω	ODT off	20Ω	na
		Slot 2	off	ODT off	20Ω	120Ω	na
SR	DR	Slot 1	off	120Ω	na	ODT off	20Ω
		Slot 2	off	20Ω	na	120Ω	ODT off
SR	SR	Slot 1	off	120Ω	na	30Ω	na
		Slot 2	off	30Ω	na	120Ω	na
DR	Empty	Slot 1	off	40Ω	ODT off	na	na
Empty	DR	Slot 2	off	na	na	40Ω	ODT off
SR	Empty	Slot 1	off	40Ω	na	na	na
Empty	SR	Slot 2	off	na	na	40Ω	na

Dynamic ODT Required

DRAM On-Die-Termination (ODT) suggestions

- READ Table for a two slot channel
  - For transfer rates of 1,066Mb/s

		READ From	Controller ODT	Slot 1		Slot 2	
Slot 1	Slot 2			Rank 1	Rank 2	Rank 1	Rank 2
DR	DR	Slot 1	75Ω	ODT off	ODT off	ODT off	30Ω
		Slot 2	75Ω	ODT off	30Ω	ODT off	ODT off
DR	SR	Slot 1	75Ω	ODT off	ODT off	20Ω	na
		Slot 2	75Ω	ODT off	20Ω	ODT off	na
SR	DR	Slot 1	75Ω	ODT off	na	ODT off	20Ω
		Slot 2	75Ω	20Ω	na	ODT off	ODT off
SR	SR	Slot 1	75Ω	ODT off	na	30Ω	na
		Slot 2	75Ω	30Ω	na	ODT off	na
DR	Empty	Slot 1	75Ω	ODT off	ODT off	na	na
Empty	DR	Slot 2	75Ω	na	na	ODT off	ODT off
SR	Empty	Slot 1	75Ω	ODT off	na	na	na
Empty	SR	Slot 2	75Ω	na	na	ODT off	na

Early Timing Budget

- READs at DDR3-1066

Element	*Skew Component*	*Setup*	*Hold*	*Units*	*Comments*
Clock	Data/Strobe chip PLL jitter	0	0	ps	*input clock jitter affects short loop timing but not data capture; except tJITper/duty below*
	DRAM tJITper	0	0	ps	*DRAM does not account for output jitter affects, must be derated*
	Clock skew	**0**	**0**	ps	
Transmitter	0.5tCK - tQH	225		ps	0.5tCK to 0.47tCK accounted for in tQHS measurement
	tDQSQ	150		ps	
	tJITduty measured, not spec	72		ps	tJITduty measured, not spec; assume 80% of tJITper
	Duty cycle adjust	-28		ps	Duty cycle improvement from WC - 48.5% and not 47%, {tCH/Lavg(min)}
	DRAM Skew	**238**	**238**	**ps**	tCK/2-(tQH+tDQSQ+duty cycle adjust+tJITper)
Interconnect	*Controller uses uncoupled package model, some increase can be expected pending Controller model used; probably in the 15ps to 30ps region				
	DQ Crosstalk and ISI*	25	25	ps	1 victim (1010...), 4 aggressors (PRBS)
	DQS Crosstalk and ISI*	5	5	ps	1 shielded victim (1010...), 2 aggressors (PRBS)
	Vref: Reduction (input eye reduction)	10	10	ps	+/- 30 mV included in DRAM skew; additional = (+/- 10 mV) / (1 V/ns)
	Path Matching (Board)	10	10	ps	Within byte lane: 165 ps/in * 0.1 in; Impedance mismatch within DQS to DQ
	Path Matching (Module)	10	10	ps	Module routing skew (30% reduction with leveling)
	Capacitance Matching	5	5	ps	strobe & data shift differently
	ODT Skew (1%)	5	5	ps	Estimated
	Total Interconnect	**70**	**70**	**ps**	
Receiver	Memory Controller Skew	**151**	**151**	**ps**	assume tDS, tDH from DRAM spec.derated for faster slew rate and to Vref
Total Loss	Total Skew	**459**	**459**	**ps**	Trans. + rec. + interconnect skew
Max Eye	**Time Allowed**	**469**	**469**	**ps**	
Budget 6L	**Timing Margin**	**10**	**10**	**ps**	6 layer board (stripline), 45-ohms, 0.135mm trace to trace spacing
6 to 4 layer	DQ Crosstalk and ISI	7	7	ps	increase using microstrip vs strip line
	DQS Crosstalk and ISI	17	17	ps	increase using microstrip vs strip line
Budget 4L	**Timing Margin**	**-14**	**-14**	**ps**	4 layer board (micronstrip) 45-ohms, 0.135mm trace to trace spacing

Early Timing Budget

- WRITEs at DDR3-1066

Element	Skew Component	Setup	Hold	Units	Comments
Clock	Data/Strobe chip PLL jitter	35	35	ps	
	DRAM tJITper	45	45	ps	*derate back out what DRAM tests for*
	Clock skew	**0**	**0**	ps	
Transmitter	**Memory Controller Skew**	**238**	**238**	**ps**	Assume similar to DRAM, used DRAM's
Interconnect	*Controller uses uncoupled package model, some increase can be expected pending Controller model used; probably in the 15ps to 30ps				
	DQ Crosstalk and ISI*	25	25	ps	1 victim (1010…), 4 aggressors (PRBS); Different termnation scheme for 800 other than that used for 1066 and 1333 should reduce xtlk to less than 25ps
	DQS Crosstalk and ISI*	5	5	ps	1 shielded victim (1010…), 2 aggressors (PRBS)
	Vref: Reduction	10	10	ps	+/- 30 mV included in DRAM skew; additional = (+/- 10 mV) / (1 V/ns)
	Reff Mismatch	0	0	ps	+/-6% accounted for by DRAM spec
	Path Matching (Board)	10	10	ps	Within byte lane: 165 ps/in * 0.1 in; Impedance mismatch within DQS to DQ
	Path Matching (Module)	10	10	ps	Module routing skew (30% reduction with leveling)
	Input Capacitance Matching	5	5	ps	strobe & data shift differently
	ODT Skew (1%)	5	5	ps	Estimated
	Total Interconnect	**70**	**70**	**ps**	
Receiver	DRAM Skew	**165**	**165**	**ps**	tDS, tDH from DRAM spec.derated for faster slew rate and to Vref
Total Loss	Total Skew	**472**	**472**	**ps**	Trans. + rec. + interconnect skew
Max Eye	**Time Allowed**	**469**	**469**	**ps**	
Budget 6L	**Timing Margin**	**-3**	**-3**	**ps**	6 layer board (stripline), 45-ohms, 0.135mm trace to trace spacing
6 to 4 layer	DQ Crosstalk and ISI	7	7	ps	increase using microstrip vs strip line
	DQS Crosstalk and ISI	17	17	ps	increase using microstrip vs strip line
Budget 4L	**Timing Margin**	**-27**	**-27**	**ps**	4 layer board (micronstrip) 45-ohms, 0.135mm trace to trace spacing

Micron

Agenda

- DDR3 RDIMM Basics and Introduction
- DDR3 RDIMM – Topology, Simulation, and Timing
  - General System Assumptions
  - Improved Topology
  - Address/Command/Control
  - Clock
  - Data
- DDR3 RDIMM – Raw Cards and Types
- DDR3 RDIMM – Early Development and Micron Support

DDR3 RDIMM – R/C Options

- JEDEC modules supported by Micron
  - SR x8 (R/C A), Micron designed
  - DR x8 (R/C B)
  - SR x4 (R/C C)
  - DR x4 stacked (R/C D)
  - DR x4 planar (R/C J)
- Additional high density modules will be offered at increased heights to address custom applications

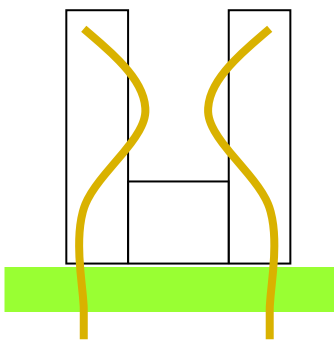
DDR3 RDIMM – R/C Options

- VLP RDIMMs
  - Most Micron modules will be available at 17.9mm overall height, currently the industry is considering 18.75mm tall maximum for VLP
    - SR x8
    - DR x8
    - SR x4
    - DR x4 stacked
- A 18.75mm tall VLP may require a custom socket to make the module fit into the ACTA form factor?

VLP RDIMMs – Sockets

- Micron supports a DDR3 17.9mm tall VLP!!!
  - Our DDR3 VLP will fit the ATCA form factor <u>with a standard socket</u> (it will fit in the custom socket too)

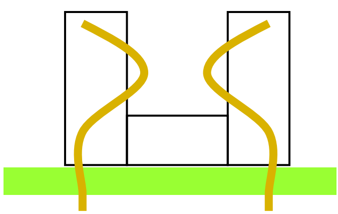
Socket for Micron VLP



Standard socket <$$$

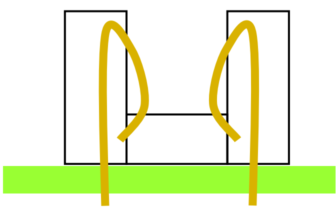
Industry Standard (short) VLP

Pending short ATCA socket (Option A)



Custom Socket will have a higher insertion force due ultra short spring connectors

Pending short ATCA socket (Option B)



Custom Socket will have a higher lead-in inductance which could severally affect high-speed functionality?

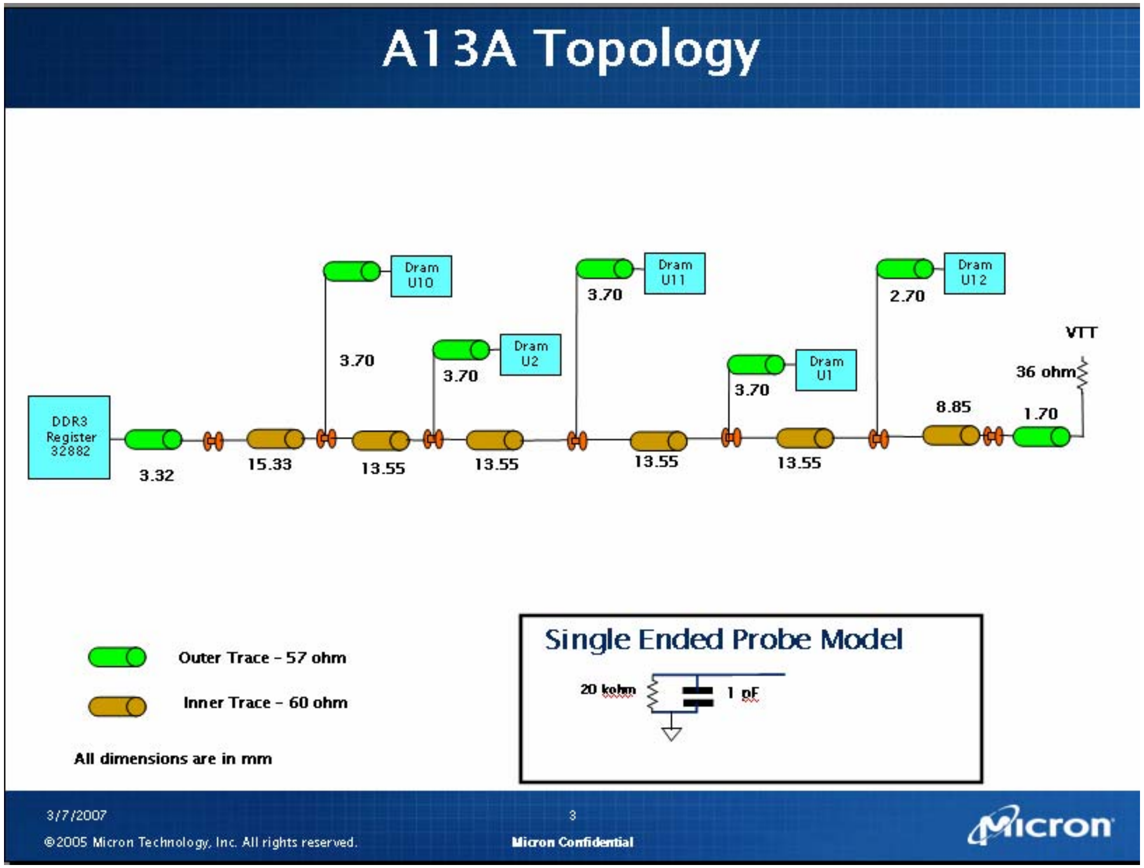
Agenda

- DDR3 RDIMM Basics and Introduction
- DDR3 RDIMM – Topology, Simulation, and Timing
  - General System Assumptions
  - Improved Topology
  - Address/Command
  - Data
- DDR3 RDIMM – Raw Cards and Types
- DDR3 RDIMM – Early Development and Micron Support

System Verification

- Micron validates our models and modules in the lab

For our DR x8 (R/C A) we have simulated with HSPICE what the A13 signal should look like if probed near DRAM location U1

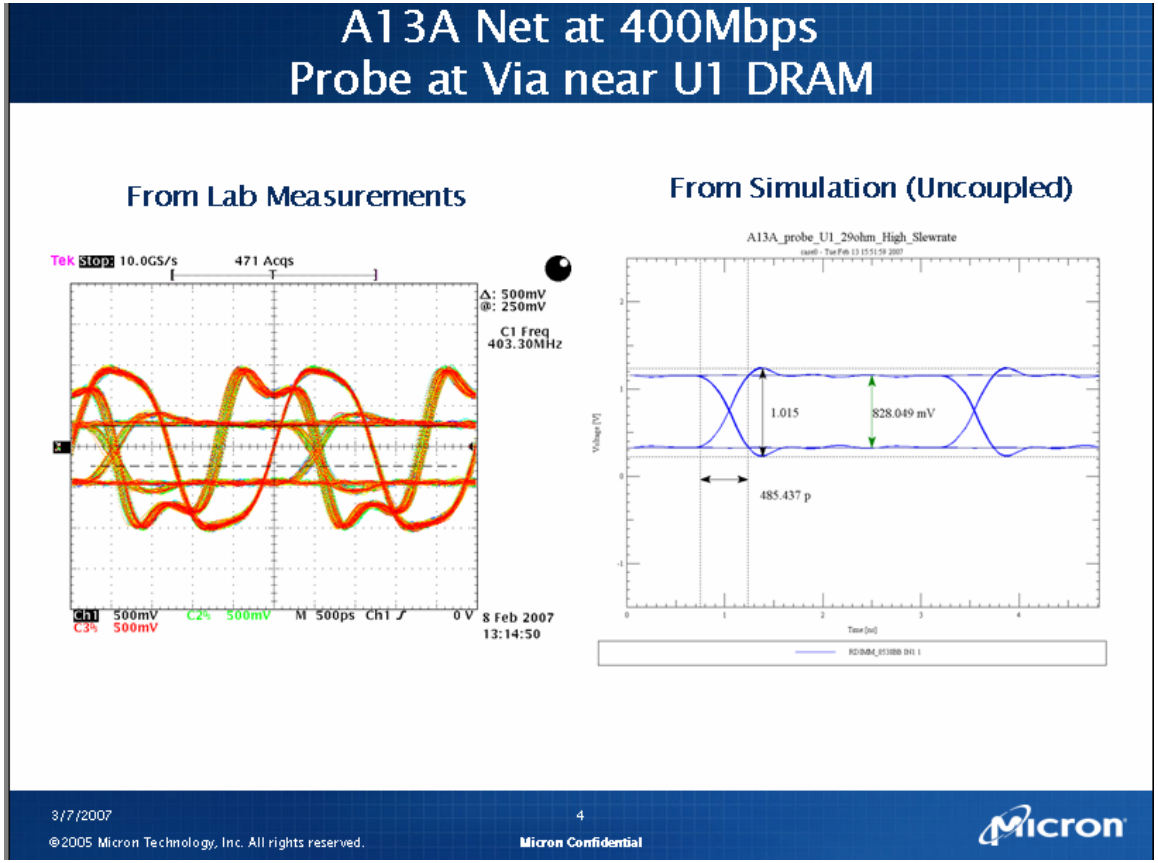


System Verification

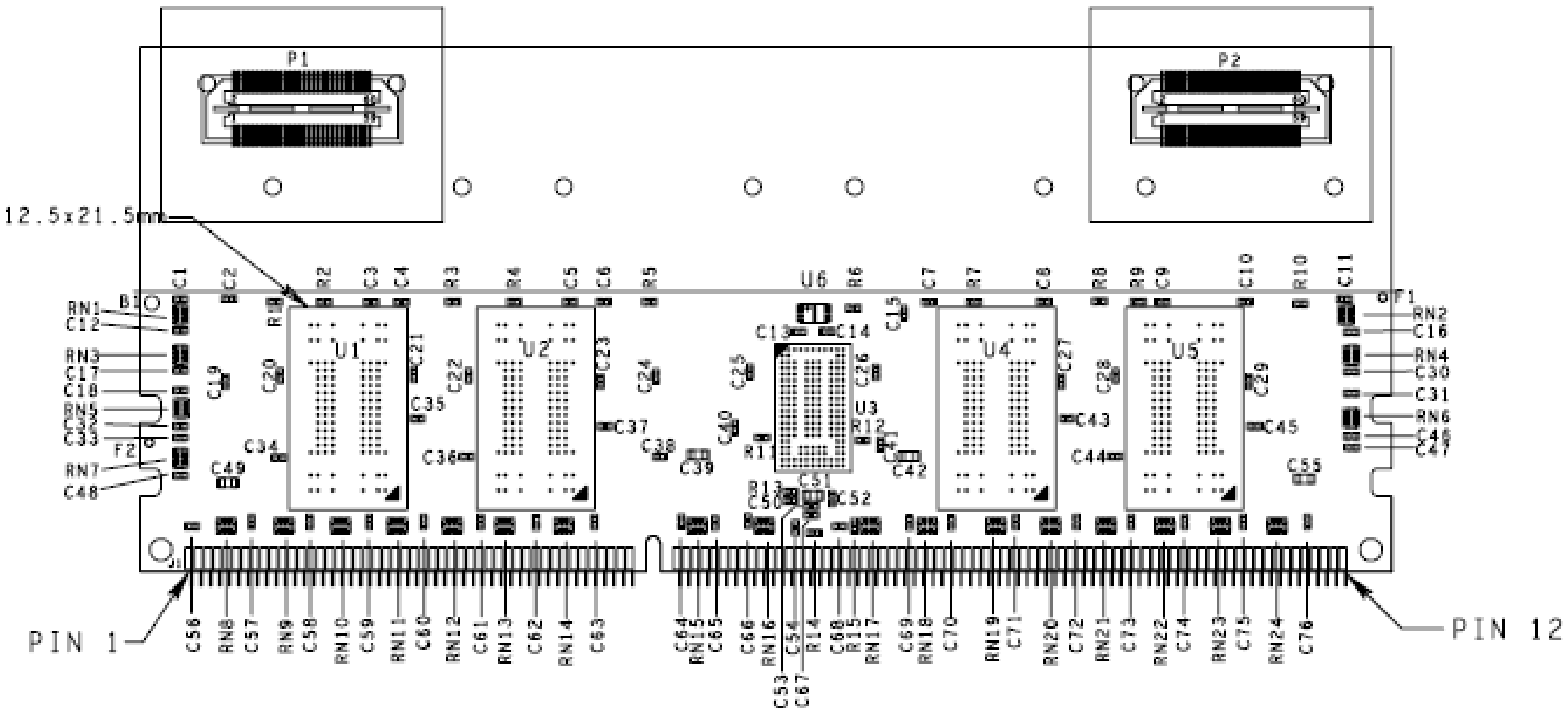
- Micron validates our models and modules in the lab

For our DR x8 (R/C A) we have simulated with HSPICE what the A13 signal should look like if probed near DRAM location U1

Then in the lab, we measure the signal to correlate our simulations



Logic Analyzer Interface Modules (Snoop DIMMs)



PRIMARY SIDE

Micron Development Tools

- Use passive probe hardware and software from NEXUS™ (http://www.nexustechnology.com/)
- Modules designed to interface to Tektronics™ Logic Analyzer
- All DQ, clock, command, control and address signals probed with no impact on module functionality
  - Micron Snoop RDIMMs available – 3Q07
    - R/C A
    - R/C C
    - R/C D

Micron®