
Microsoft
WinHEC
2007

Main Memory Technology Direction

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Agenda

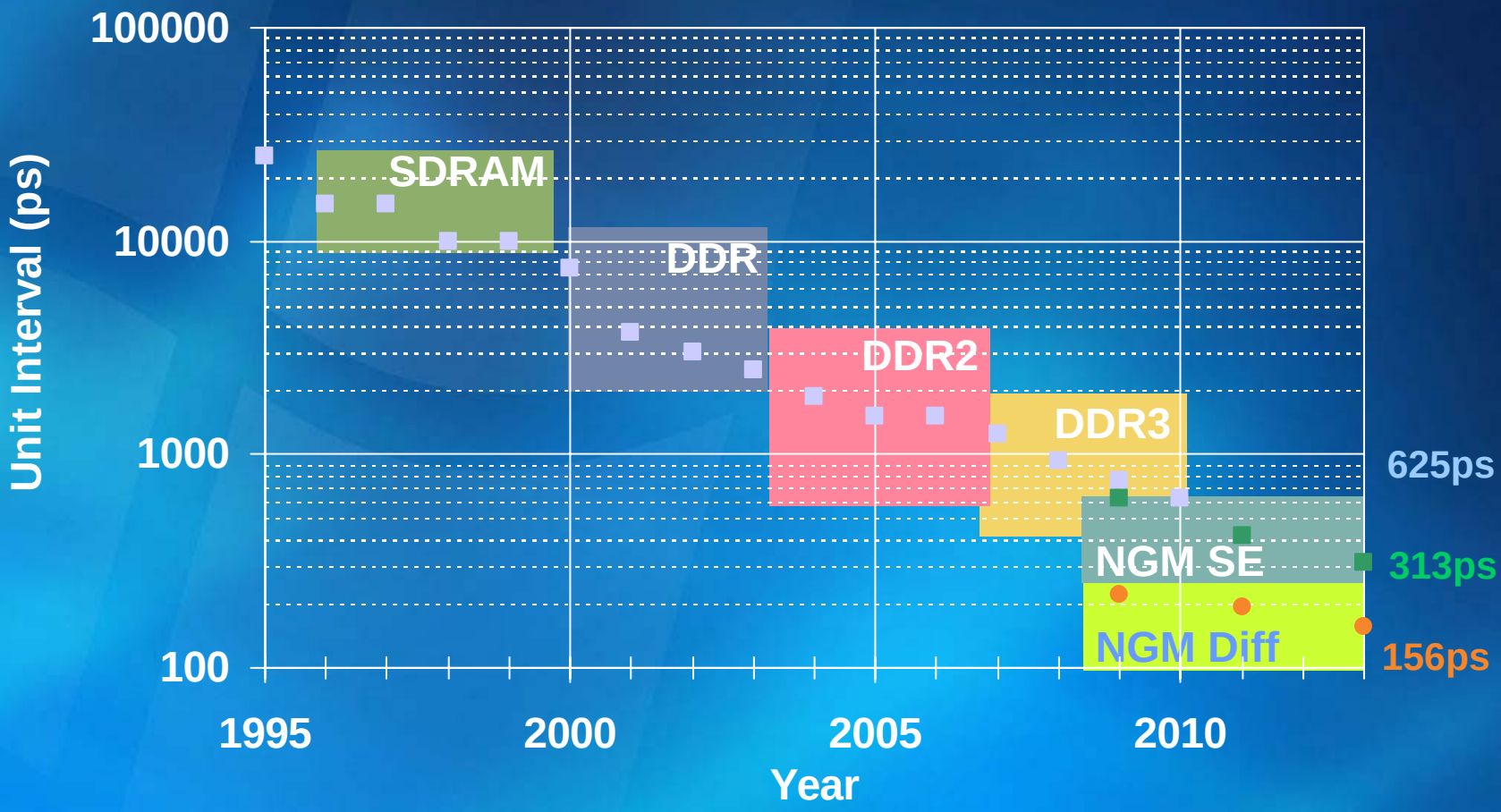
- DRAM Technology Trends
- Computing Customer Requirements
- Introduction to DDR3

DRAM Technology Trends

Main Memory Data Rate Trends

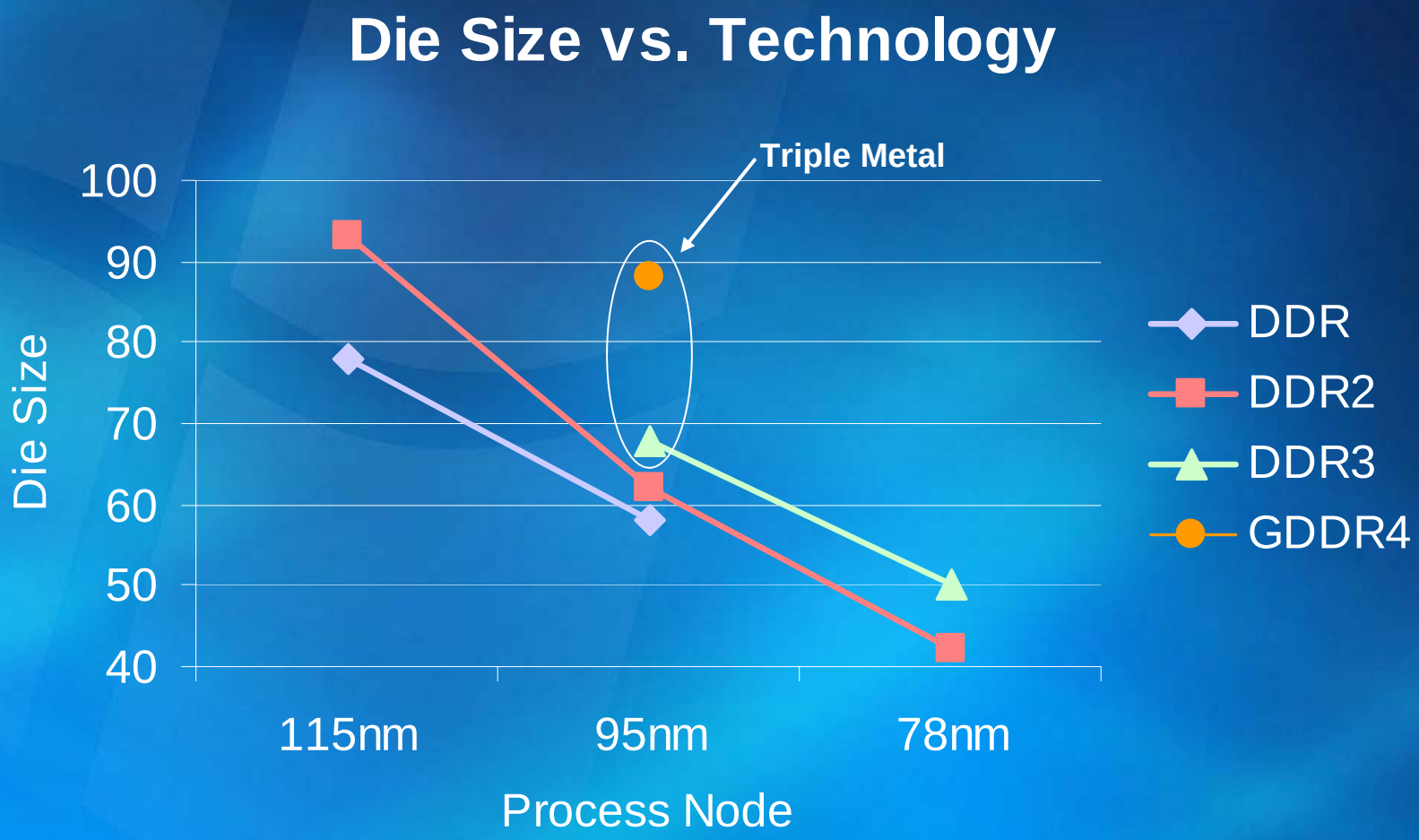
- DRAM bandwidth requirements typically double every three years

Unit Interval (Bit-Time) Trends



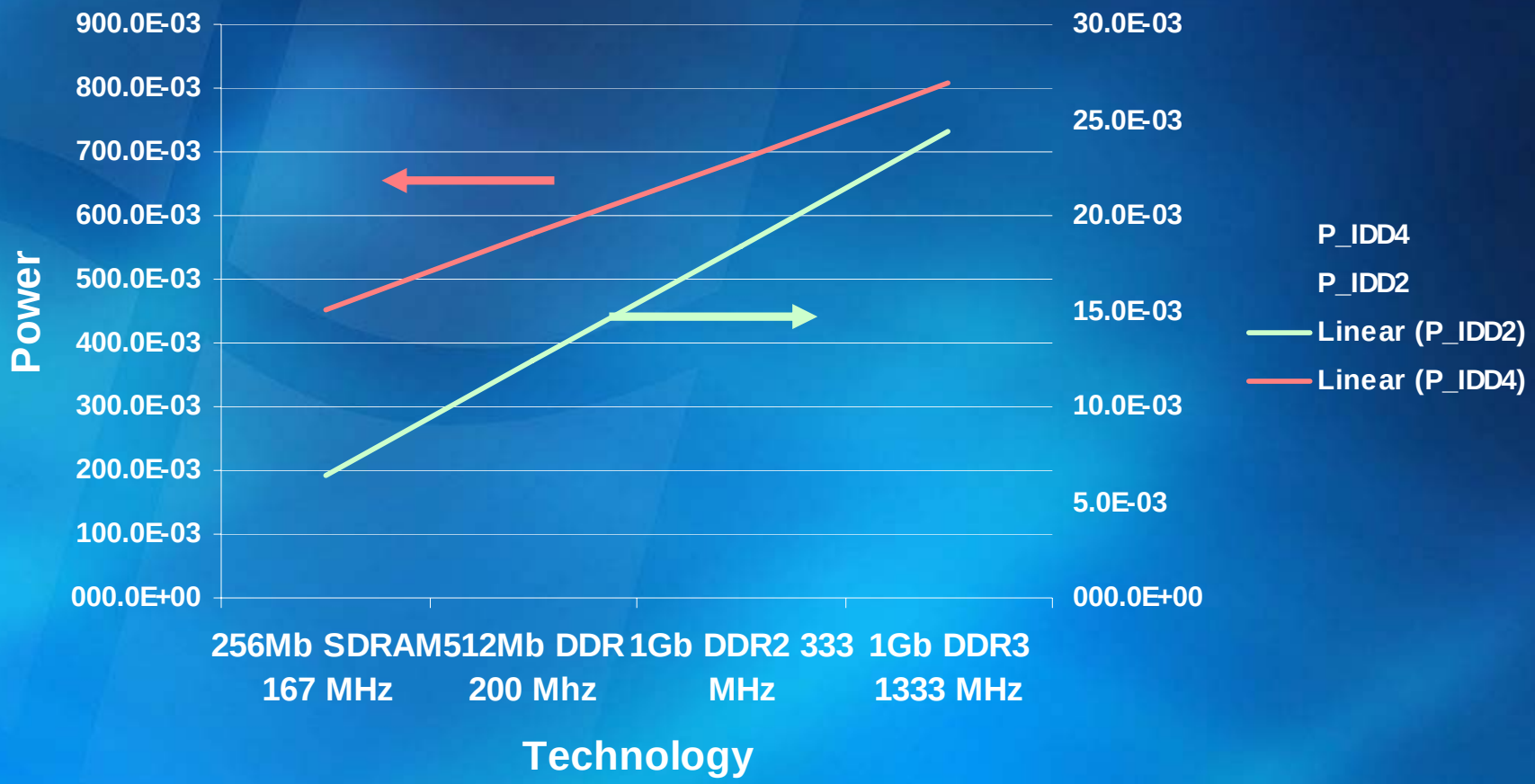
- 30–40% of UI will be budgeted for RX circuits (jitter + S/H + static)

Die Size Impact



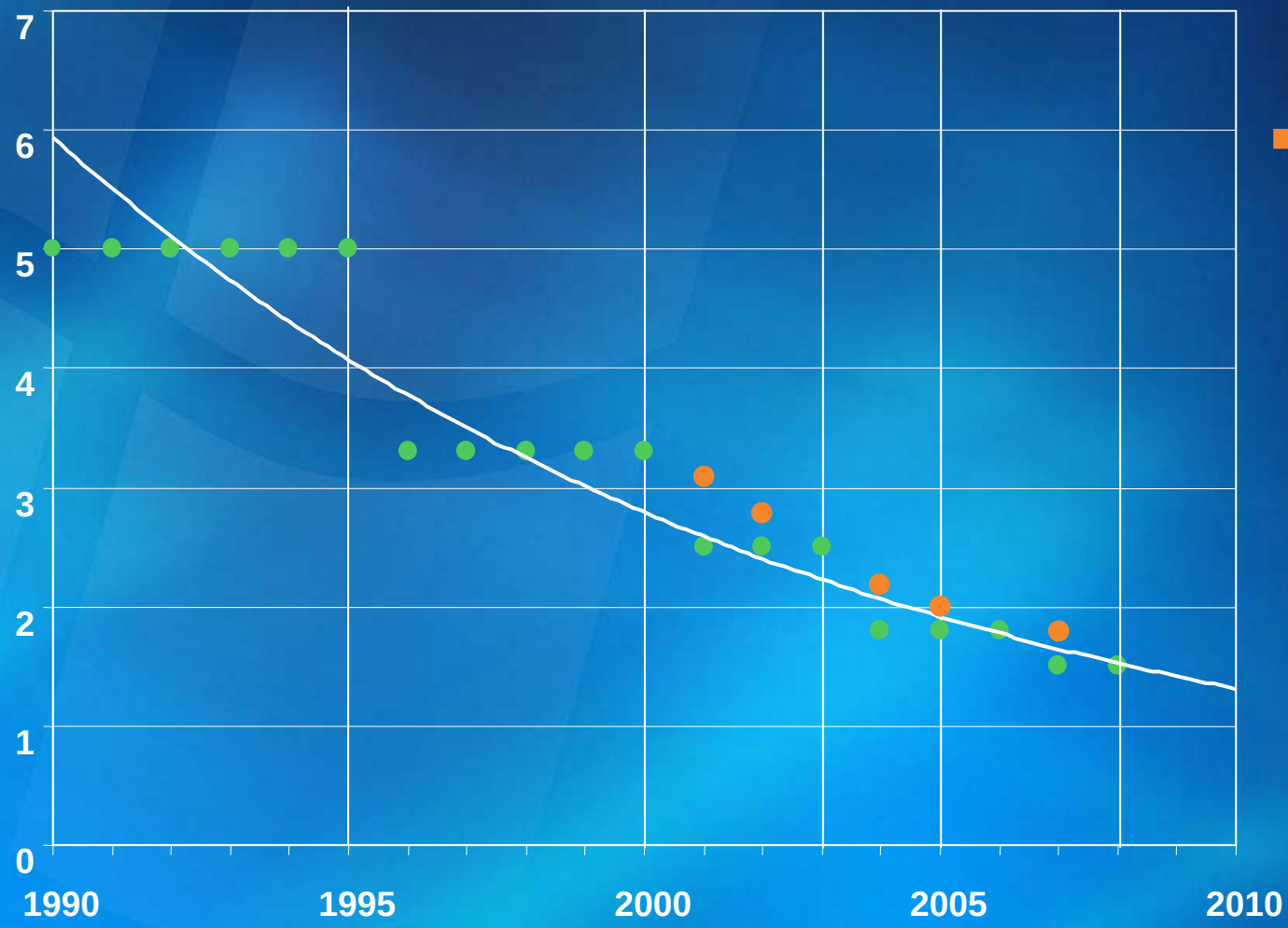
IDD Impact

Power Dissipation Trends

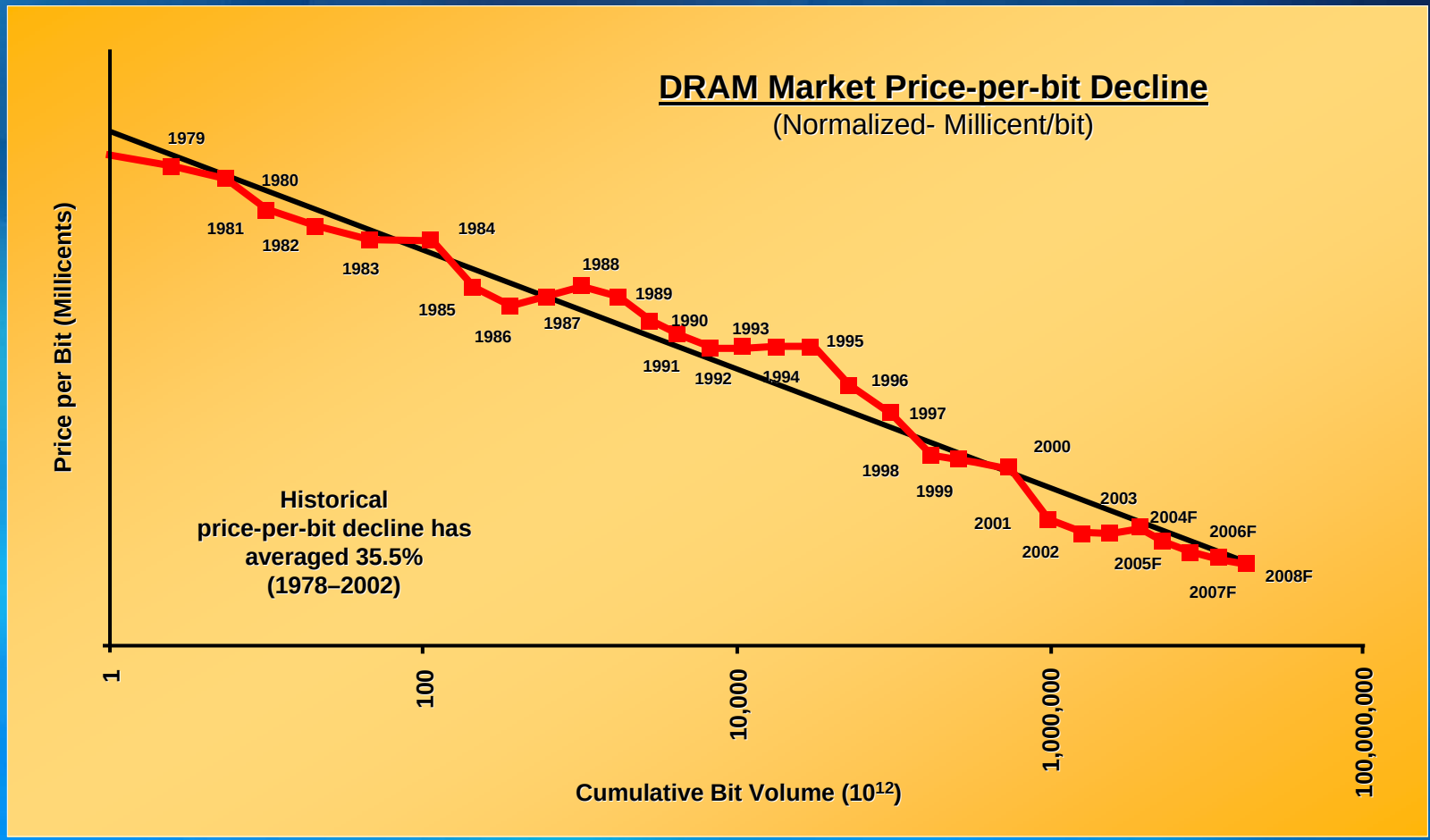


- x16 devices at nominal V_{DD}

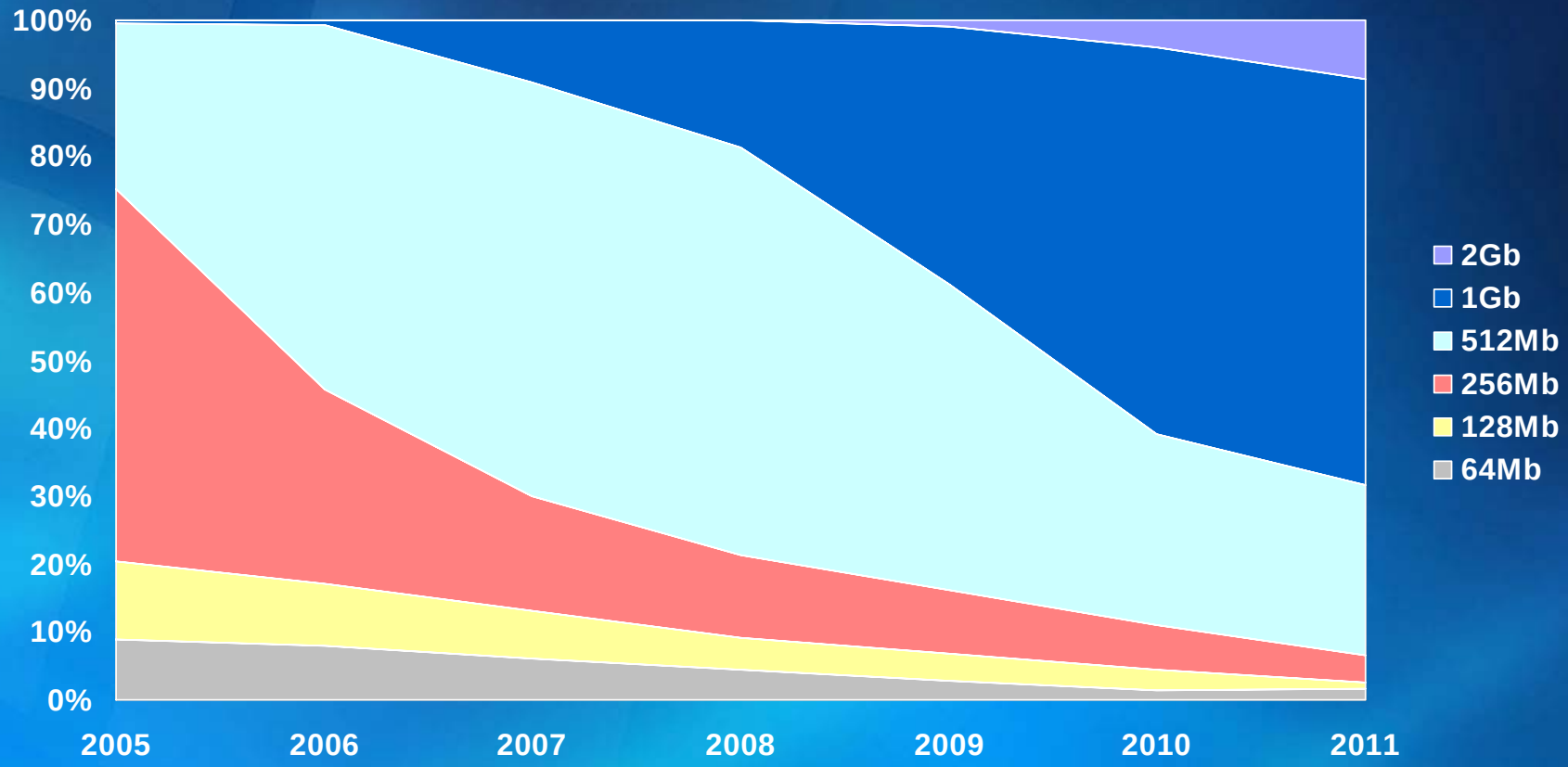
Voltage Scaling



Historical DRAM Price-Per-Bit Decline ~35%/year

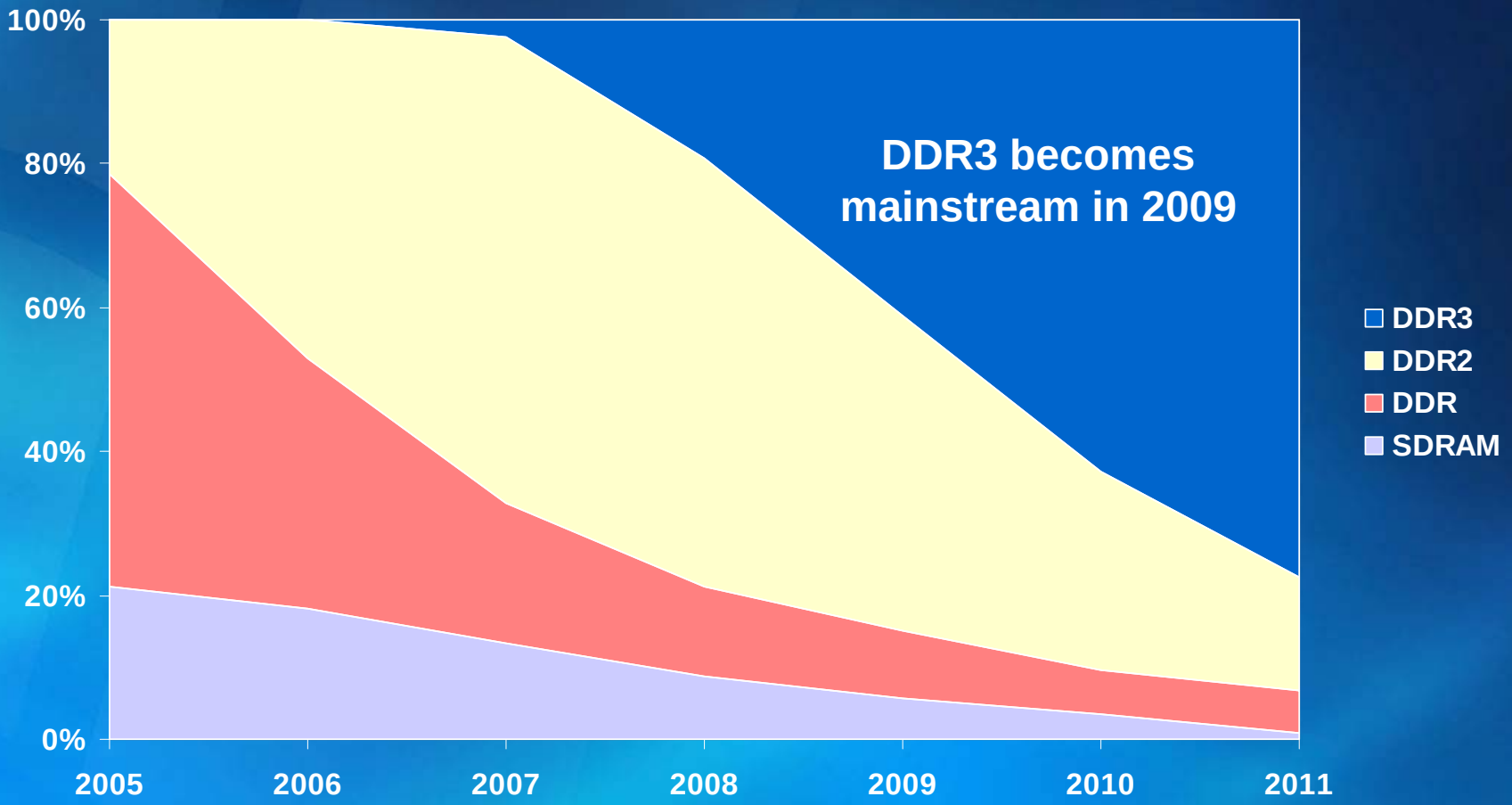


Industry Analyst DRAM Interface Forecast



Source: IDC, Isuppli, Gartner, Micron Q107

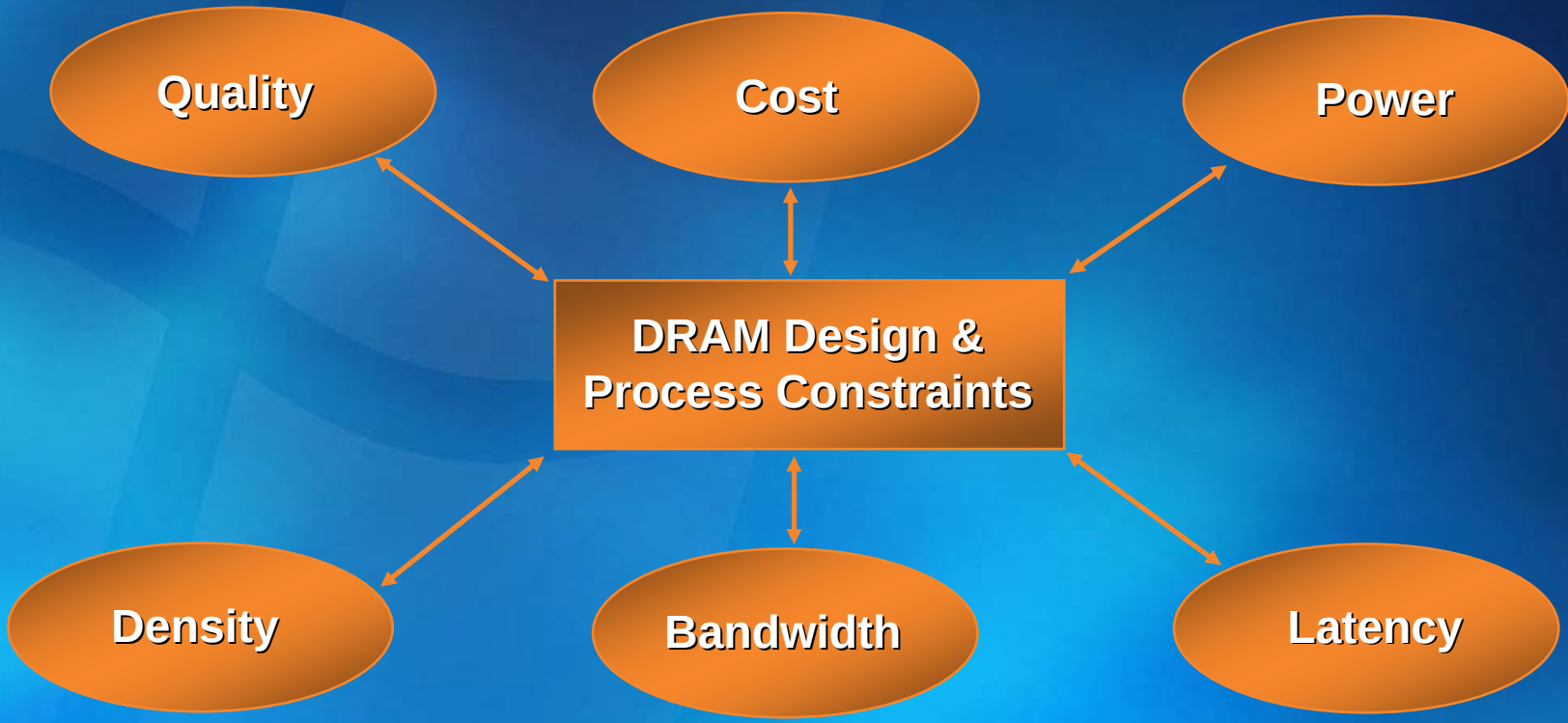
Industry Analyst DRAM Interface Forecast



Source: IDC, iSuppli Q107

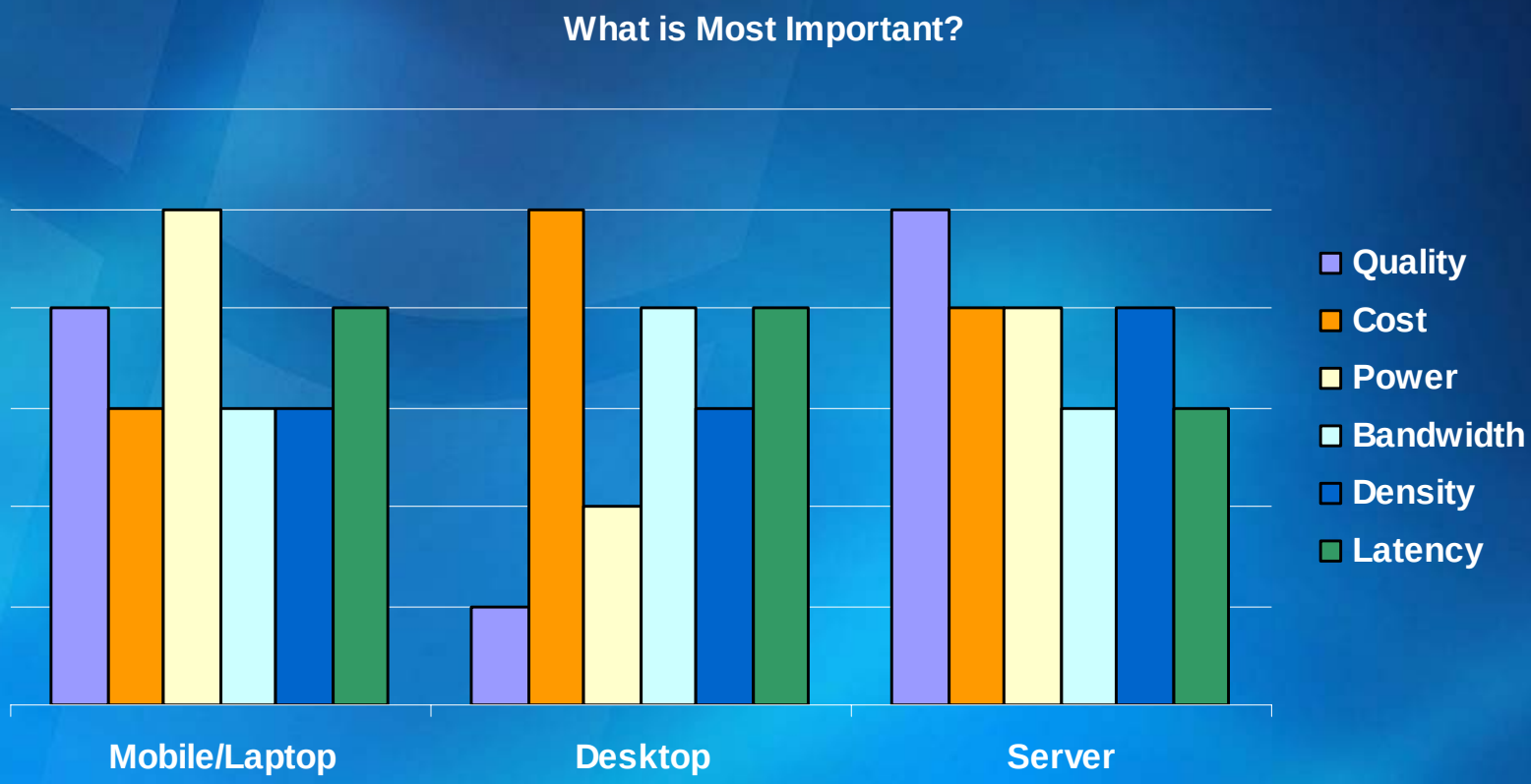
Computing Customer Requirements

You Can't Have It All

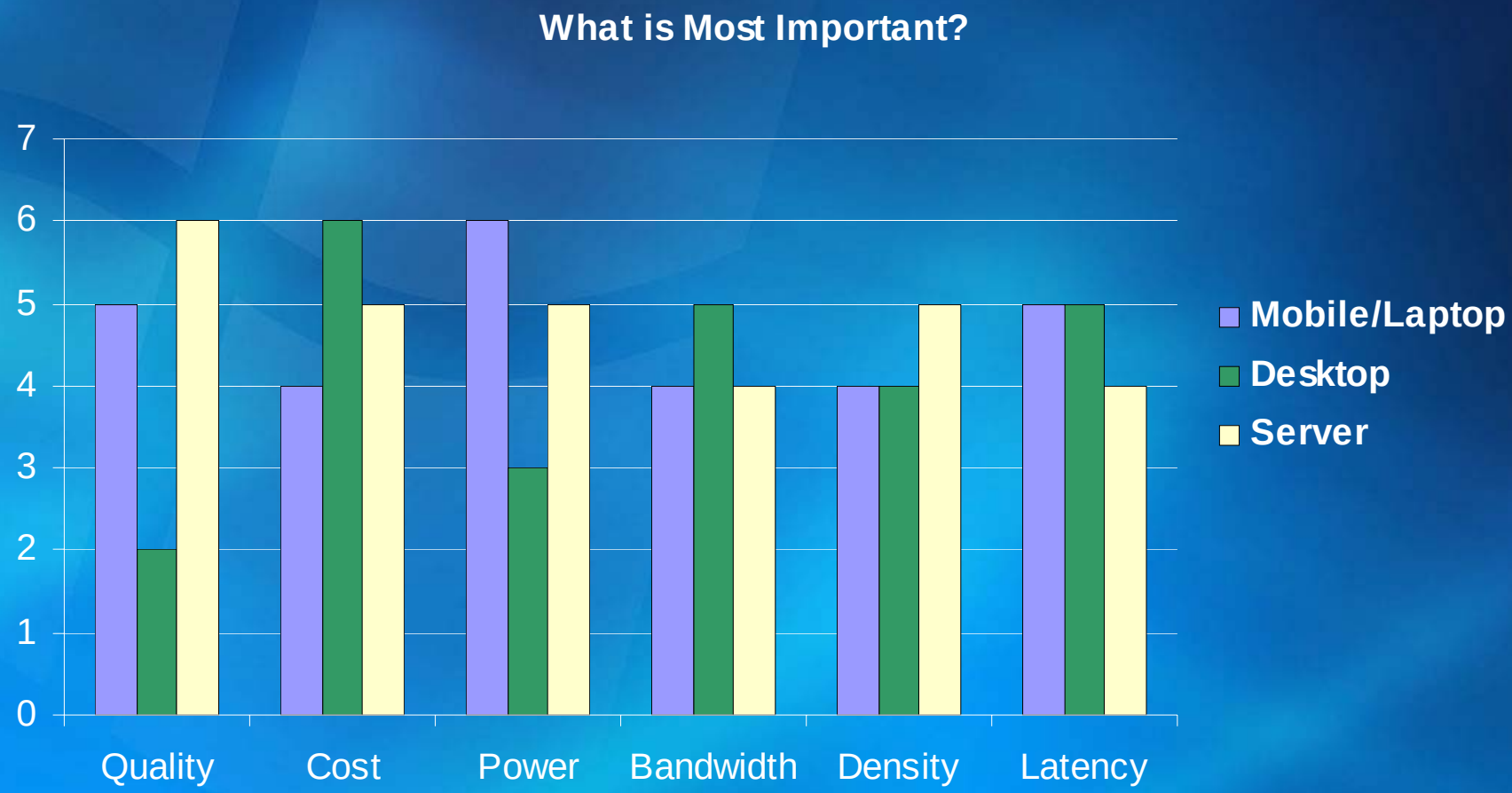


- Pick two (maybe three if you're really lucky!)

What Computing Customers Care About



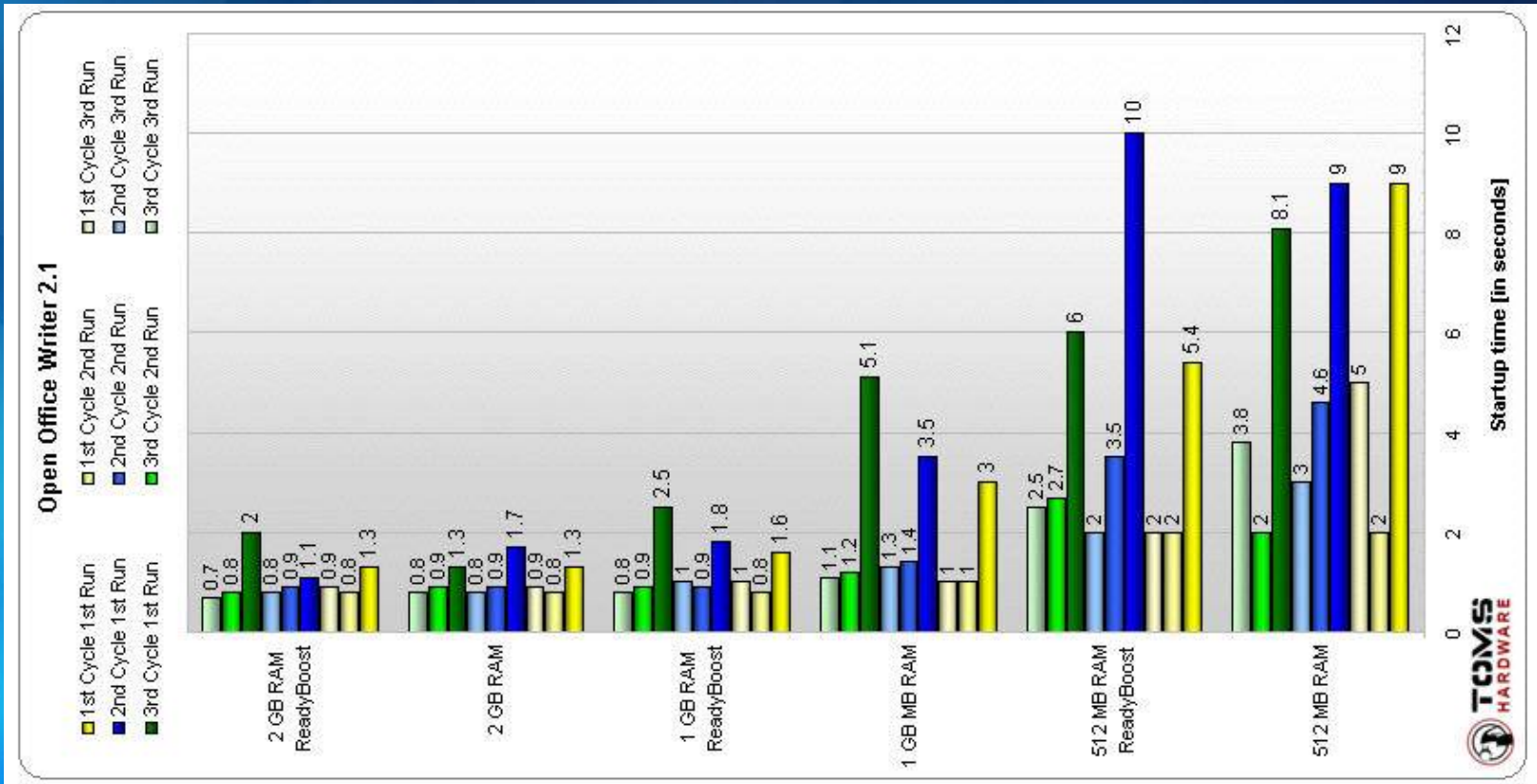
What Computing Customers Care About



Microsoft's Vista System Requirements

	Minimum Supported	Minimum Recommended by SKU	
		Home Basic	All Other SKUs
CPU	An 800 MHz x86 or x64 processor[3]		A 1 GHz x86 or x64 processor[3]
System memory	512MB		1GB
GPU	SVGA (800 x 600)	DX9 Capable	Aero-capable
Graphics memory		32MB	128MB [1, 2]
HDD	20GB		40GB
HDD free space	15GB		
Optical drive	CD-ROM[4]	DVD-ROM[4]	
Networking		Internet access-capable	
Audio		Audio output capability	

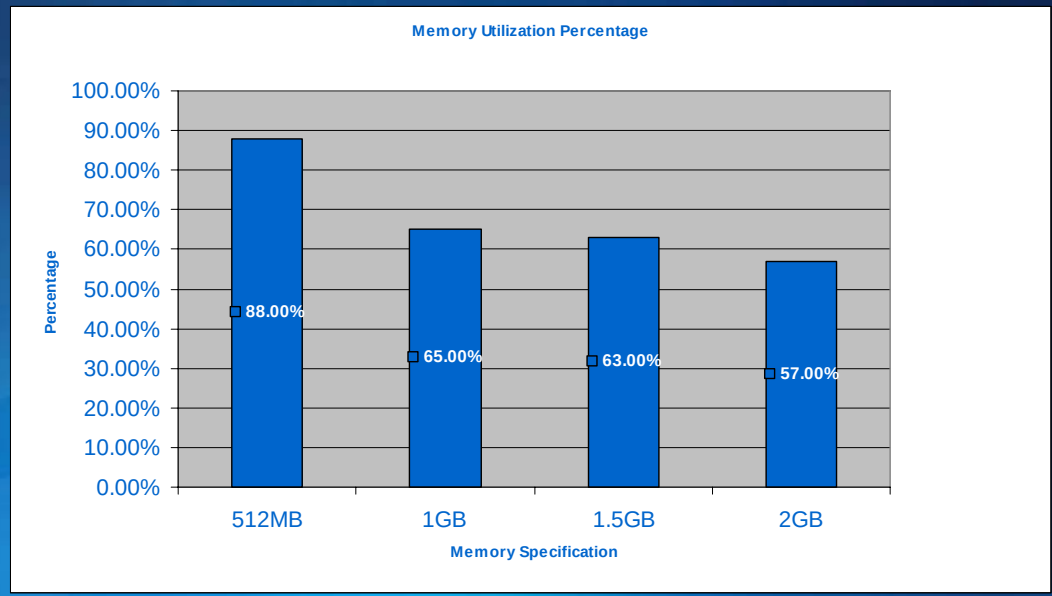
Density Matters



- "Give Vista as much memory as you can, and it will thank you by serving you quicker."
  - Tom's Hardware, Windows Vista's SuperFetch and ReadyBoost Analyzed, January 31, 2007
  - http://www.tomshardware.com/2007/01/31/windows-vista-superfetch-and-readyboostanalyzed/index.html

Windows Vista RTM Test Results

- Memory utilization is minimized with more system memory installed
- SuperFetch exhausts DRAM memory before using NAND memory
  - 2GB appears to be optimal DRAM density for Vista
- Multiple programs running
  - Two Web browsers, Windows Media Player, Adobe Photoshop with 445MB file open, and Trend Virus Protection



Lower number means your system has more resources available for additional tasks

System Specifications

Inspiron 6000
Intel 915GM/PM
Vista RC2

Intel Pentium M 1.7 Ghz
ATI Mobility Radeon X300
80GB Fujitsu ATA

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Vista Ready Boost C&P Lab Results

- With 2x CT3264AA667 512MB of DRAM installed:

Ready Boost disabled	Ready Boost enabled
1:20.04	38.23 sec
1:09.48	33.23 sec
1:15.56	29.81 sec
1:06.06	44.46 sec

- With 2x CT6464AA667 1024MB of DRAM installed:

Ready Boost disabled	Ready Boost enabled
8.39 sec	7.43 sec
8.18 sec	7.29 sec
8.56 sec	6.50 sec
7.81 sec	7.51 sec

Vista Ready Boost C&P Lab Results

- With 2x CT12864AA667 2048MB of DRAM installed:

Ready Boost disabled	Ready Boost enabled
6.73 sec	5.57 sec
5.93 sec	5.14 sec

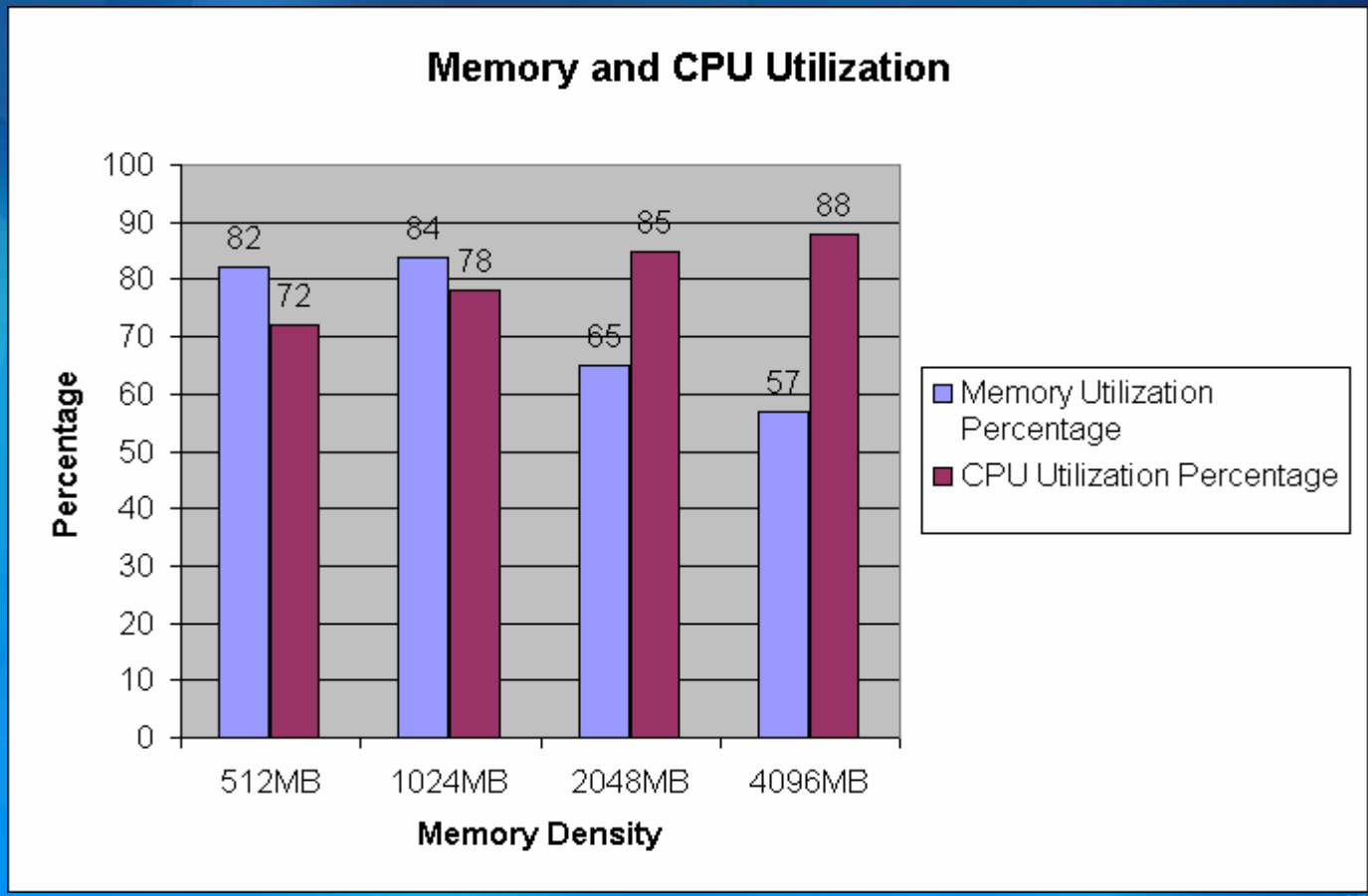
- With 4x CT12864AA667 4096MB of DRAM installed:

Ready Boost disabled	Ready Boost enabled
21.21 sec	7.07 sec
5.48 sec	6.29 sec

- 2GB DRAM achieves the peak performance gain for DRAM density in Vista systems using Ready Boost

DRAM Density Increases CPU Efficiency

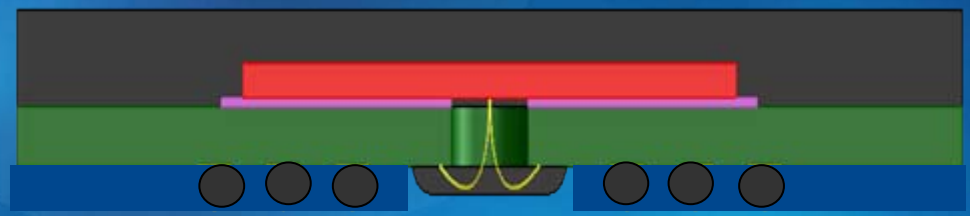
- As memory density increases, memory utilization decreases
- As memory density increases, processor utilization goes up
- More memory drastically increases the efficiency of your processor



System Specifications Motherboard: Evga NF68 Chipset: nVidia 680i SLI Processor: Intel Pentium 4 2.8GHZ Video: ATI Radeon X1900XTX PCIE 512MB Hard Drive:WD 80GB OS: Windows Vista Ultimate DRAM: Crucial DDR2 6400 Real World Test Processes running to generate utilization: Nero Recode, ADOBE WITH 445 MEG FILE OPEN, 2 WEBSITES OPEN

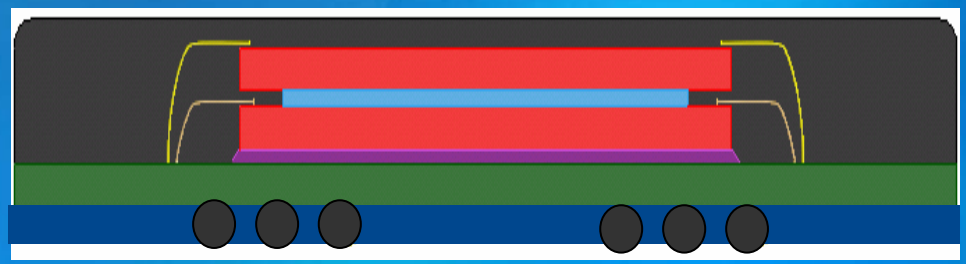
Dual-Die Stacking Technology

- Typical monolithic FBGA packages utilize BOC (board-on-chip) technology



- Typical dual-die FBGA packages utilize COB (chip-on-board) technology

1.2mm thick

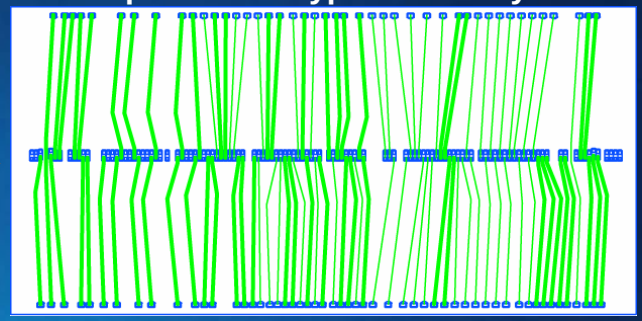


Supports DDR3 data rates

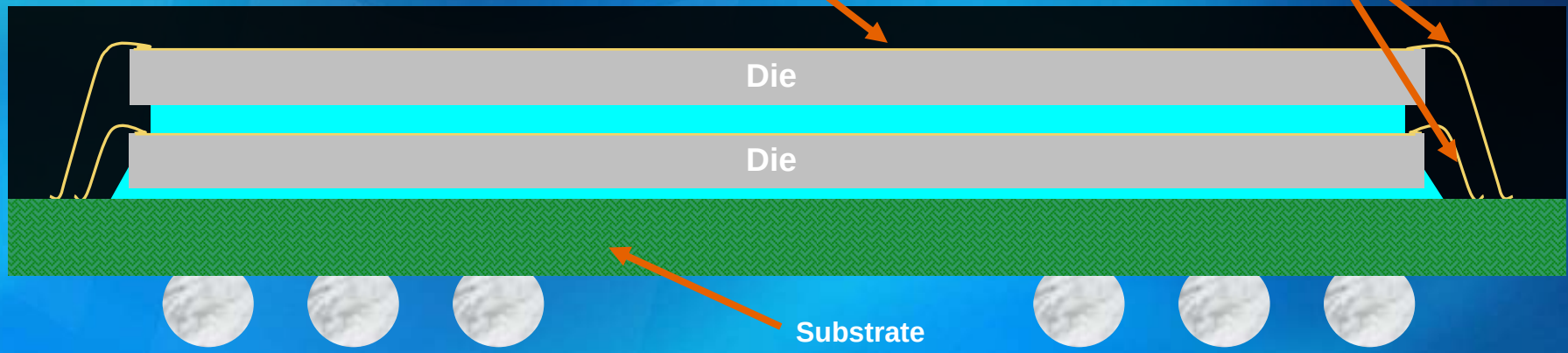
Dual-Die Package Construction

- Maximum Thickness = 1.35mm

Top view of a typical RDL layer

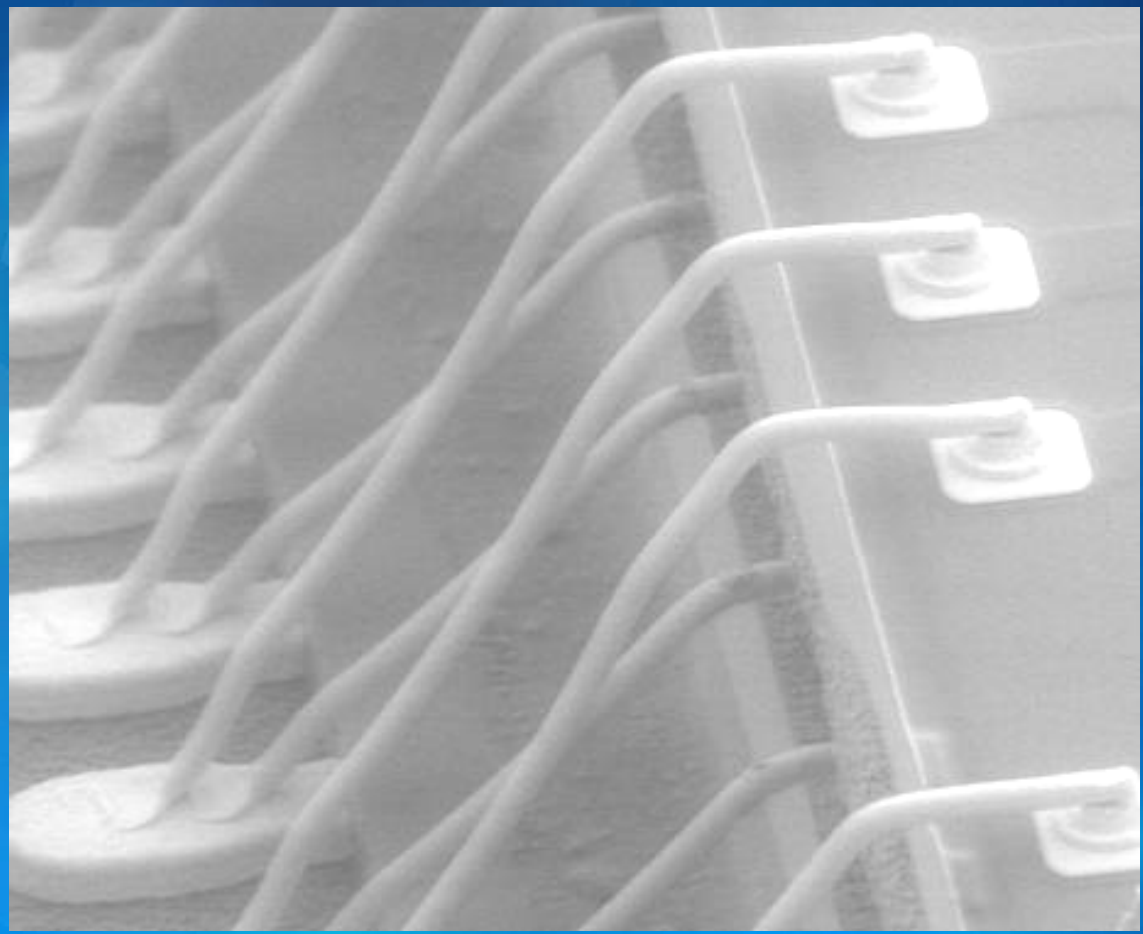


RDL = Redistribution layer; center wire bond pads are redistributed to perimeter of die through a metal layer to facilitate stacking



Dual-Die Photo

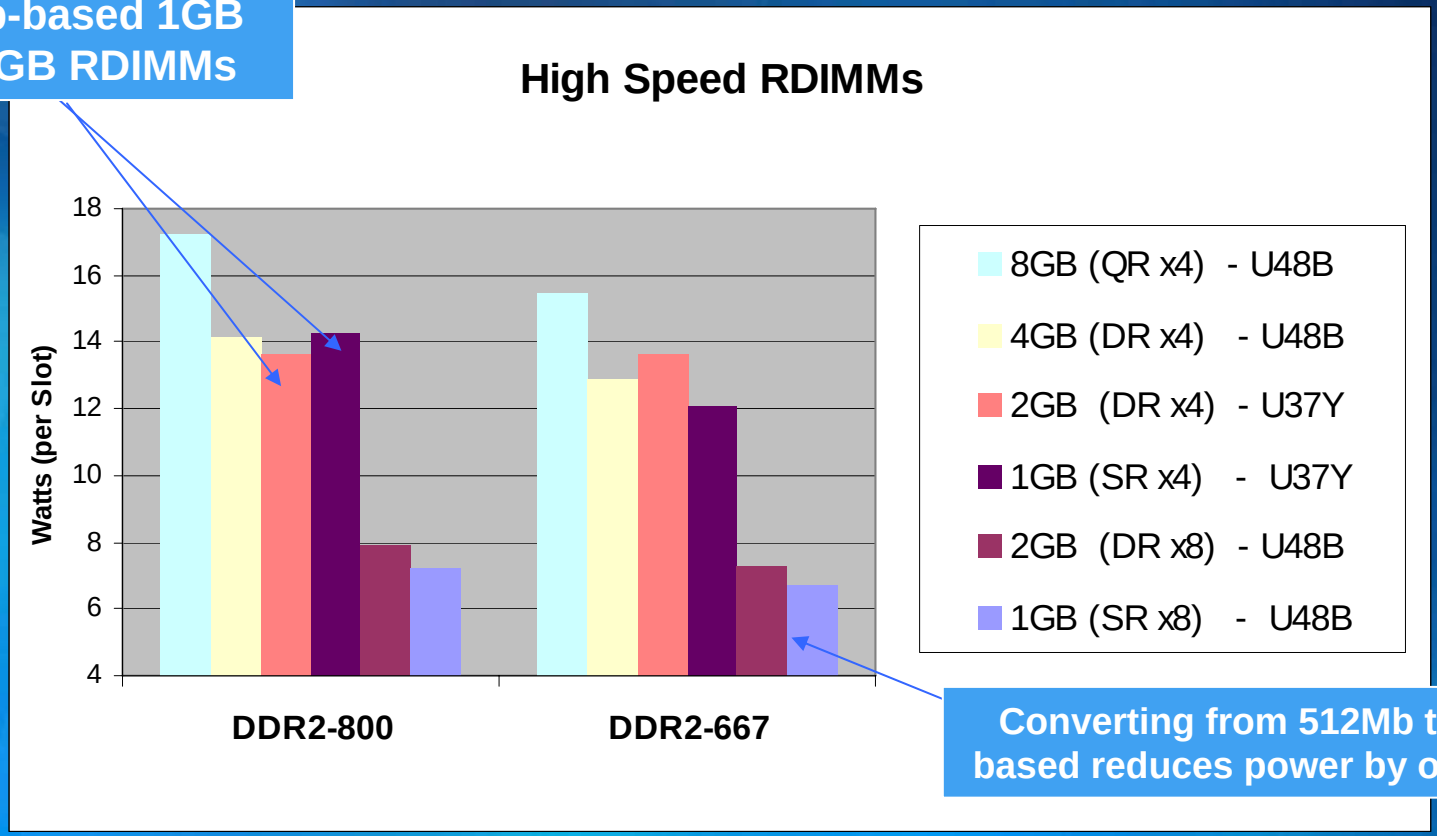
- Two die complete with wire bond prior to encapsulation



Power Consumption

4X density increase with little to no power increase

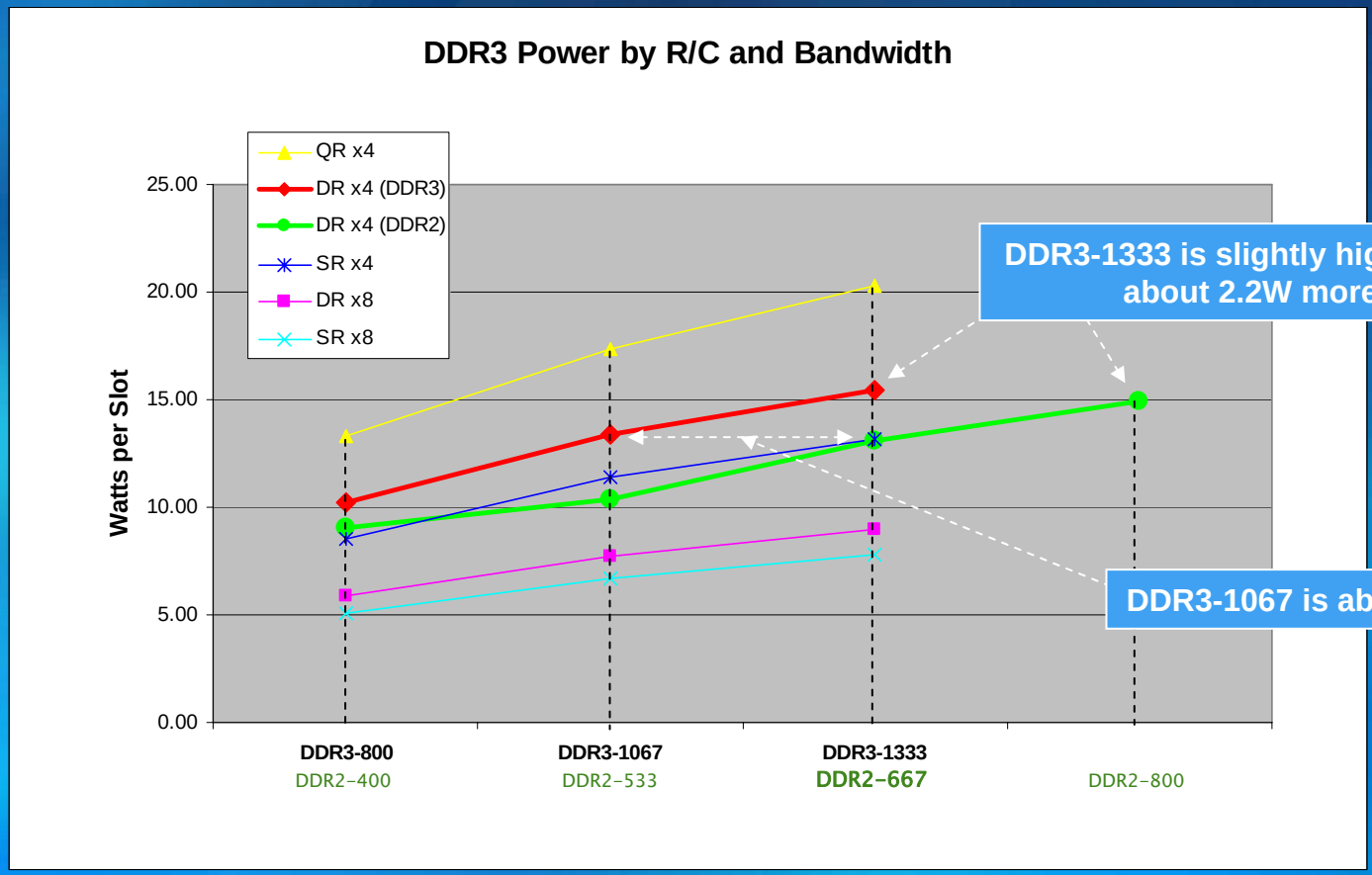
512Mb-based 1GB and 2GB RDIMMs



Converting from 512Mb to 1Gb-based reduces power by over 50%

- **Power estimates reflect a maximum DRAM utilization of 67% with a BL = 4 and register/PLL power of 1.5W**

Estimated WC power
Using (1Gb) Datasheet Values



DDR3-1333 is slightly higher than DDR2-800 and about 2.2W more than DDR2-667

DDR3-1067 is about equal to DDR-667

DDR3 (DR x4)

DDR2 (DR x4)

Reflects a sustained channel bandwidth of 65% maximum DRAM, 2x READs to WRITEs distributed evenly through all ranks, closed page, single slot populated, PLL/register package included

Introduction to DDR3

DDR2 to DDR3 Comparison
Standard Features

Features/Options	DDR2	DDR3	Comments
Pin-out/Package	60-ball; x4, x8 84-ball; x16 FBGA only	78-ball; x4, x8 96-ball; x16 FBGA only	Independent pin-out for x4/x8 and x16 (simplifies module design)
Voltage	1.8V 1.8V I/O	1.5V 1.5V I/O	Reduces memory system power demand
Densities	256Mb–4Gb	512Mb–8Gb	High-density components enable large capacity memory subsystems
Internal banks	4 (256Mb, 512Mb) 8 (1Gb, 2Gb, 4Gb)	8 (512Mb, 1Gb, 2Gb, 4Gb, 8Gb)	Larger density per monolithic package, 8 banks is standard
Prefetch (MIN READ burst)	4-bit (2 clocks)	8-bit (4 clocks)	Reduced core speed dependency for better yield
^{t}CK – DLL enabled	125 MHz to 400 MHz	300 MHz to 800 MHz	Supports higher data rates

DDR2 to DDR3 Comparison
Standard Features

Features/Options	DDR2	DDR3	Comments
Burst length (BL)	BL4, BL8	BC4, BL8	BC4 provides relief from some “BL8” requirements
Burst type	Fixed, via LMR	(1) Fixed, via MRS (2) OTF, “on-the-fly”	OTF allows switching between BC4 and BL8 without MRS command
Speed (data pin)	400, 533, 667, 800 Mb/s	800, 1066, 1333, 1600 Mb/s	Migration to higher-speed I/O
Additive Latency (AL) (Posted CAS)	AL options (0, 1, 2, 3, 4)	AL options 0, CL - 1, CL - 2	Mainly used in server applications to improve command bus efficiency
READ Latency	AL + CL CL = 3, 4, 5, 6	AL + CL CL = 5, 6, 7, 8, 9, 10	800(-25E) 5-5-5 1333(-15F) 8-8-8 800(-25) 6-6-6 1333(-15E) 9-9-9 1066(-187E) 7-7-7 1600(-125E) 9-9-9 1066(-187) 8-8-8 1600(-125) 10-10-10
WRITE Latency	RL - 1	AL + CWL CWL = 5, 6, 7, 8	Reduces latency combinations, one latency per ^{t}CK range

DDR2 to DDR3 Comparison
Standard Features

Features/Options	DDR2	DDR3	Comments
Data strobes	Single-ended or differential	Differential only	Reduce data strobe crosstalk
Data bus termination Rtt	on-die termination (ODT) opt. on MB	on-die termination (ODT) opt. on MB	Optimized for higher data rates
Rtt values	50, 75, 150 ohm	120, 60, 40, 30, 20 ohm	Support higher data rates
Rtt allowed	Read, writes, standby	Writes, standby	DDR3 does not allow during reads
Dynamic ODT	None	120, 60 ohm	Supports 2-slot; writes only
DQ driver impedance	18 ohm	34 ohm	Optimized for 2-slot and pt-to-pt systems
Driver/ODT calibration	None	External resistor	Improves accuracy over voltage and temperature

DDR2 to DDR3 Comparison
Standard Features

Features/Options	DDR2	DDR3	Comments
Multi-purpose register (MPR)	None	Four registers – 2 defined, 2 RFU	Provides specialty readouts
Write leveling	None	DQS captures CK, DQ drives out CK's state	De-skews fly-by layout used by modules
RESET#	None	Dedicated input	Disable outputs, resets DRAM
Modules	240-pin UDIMM, RDIMM, FBDIMM; 200-pin SODIMM	240-pin UDIMM; RDIMM and FBDIMM TBD; 204-pin SODIMM	Similar dimensions as DDR2

DDR2 to DDR3 Comparison
Optional Features

Features/Options	DDR2	DDR3	Comments
Automatic self refresh (ASR)	None	Optional	Automatically adjust refresh rate during self refresh mode
^{t}CK – DLL disabled	Undefined (optional)	128 kHz to 125 MHz (optional)	Provides some guidance for DLL disabled mode, if supported
ODTS, via MPR (On-die temp sensor)	None	2 readout points (3 states – 1X, 2X, >2X refresh rate), optional	ODTS to trip at refresh points, with 2C grace margin. 85C, 95C

DDR3 Performance Timeline

- DDR3 data rate and latency timeline

2007			2008			2009		
Speed	Latency	^{t}AA (ns)	Speed	Latency	^{t}AA (ns)	Speed	Latency	^{t}AA (ns)
1067	CL7	13.125	1333	CL8	12	1600	CL10	12.5
	CL8	15		CL9	13.5	1333	CL8	12
800	CL5	12.5	1067	CL7	13.125		CL9	13.5
	CL6	15	800	CL5	12.5	1067	CL7	13.125

- Fastest speed grade driven by high-end desktop
- Mainstream will not pay for speed
- Notebook and server segments tend to follow mainstream desktop
- 15ns latencies not expected to be required for 1333 and above

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