

Leverage Existing RLDRAM[®] 2 and DDR3 PHY to Design in New RLDRAM 3 2Q11



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Micron's RLDRAM 3 PHY Strategy

Use existing technologies to improve
RLDRAM 3 time-to-market without compromising performance

Leverage RLDRAM 2

- Command protocol
- SDR addressing
 - *Multiplexed/non-multiplexed*
- Free-running differential input and output strobes and QVLD signal
- Low bus turnaround time
- Burst length availability: 2, 4, 8
- Boundary scan

Leverage DDR3

- SSTL-based I/O
- ZQ-calibrated output drive and ODT
- Same speed bin cadence
 - 1600, 1866, 2133 Mb/s
- AC timing¹
 - Skews, slew rates, jitter, derating
- Read training register
- RESET pin

Note: 1. Not all AC timing is the same; leverages DDR3 jitter, skew, slew rates, and derating where applicable.

RLDRAM 3 and DDR3 PHY Features

Feature	RLDRAM 3	DDR3	Comments
Command Pins	WE#, REF#, CS#	RAS#, CAS#, WE#, CS#	RLDRAM 3 uses same command protocol and closed page architecture as RLDRAM 2
Addressing	<ul style="list-style-type: none"> • SDR-based • 4-bank address • 18–20 addresses (non-MUX) • 11 addresses (MUX) 	<ul style="list-style-type: none"> • SDR-based • 3-bank address • 13–15 addresses (MUX) 	Varying number of address pins based on density, burst length, and configuration
Data Strobes	Free-running differential write/read strobes (DK/DK#[0:1]; QK/QK#[0:3]; QVLD[0:1])	Differential shared write/read strobes (LDQS/LDQS#; UDQS/UDQS#)	RLDRAM 3 uses same data strobe methodology as RLDRAM 2; per-byte QK strobes plus additional QVLD for x36
I/O	SSTL 1.2	SSTL 1.5 (and SSTL 1.35)	Similar I/O scaled for voltage
Output Driver	240Ω based p-chan pull-ups and n-chan pull-downs	240Ω based p-chan pull-ups and n-chan pull-downs	Same I/O structures; impedance value selected through mode register
ODT	“Intelligent” No external pin; turns off automatically during read	External pin needed to turn off manually during read	ODT shared with output driver on both designs for reduced pin cap; termination value selected through mode register

RLDRAM 3 and DDR3 PHY Features (cont'd)

Feature	RLDRAM 3	DDR3	Comments
ZQ Pin	External 240Ω resistor used for calibration	External 240Ω resistor used for calibration	Calibrates driver and ODT; identical calibration scheme
Training	Read training register	Multipurpose register	Same functionality; more robust data patterns in RLDRAM 3
Voltages	$V_{DD} = 1.35V$ $V_{DDQ} = 1.2V$ $V_{EXT} = 2.5V$ $V_{REF} = V_{DDQ}/2$	$V_{DD} = 1.5V, 1.35V$ $V_{DDQ} = 1.5V, 1.35V$ $V_{REF} = V_{DDQ}/2$	V_{EXT} for array access transistor on RLDRAM 3 (same as RLDRAM 2)
Speed Bin Cadence	1600, 1866, 2133 Mb/s	1066, 1333, 1600, 1866, 2133 Mb/s	Same high-end speed bins use same skew, slew rate, jitter, and derating specs
RESET Pin	Included	Included	Same functionality
Data Masking	Upper and lower DM pins	Upper and lower DM pins	Same functionality

