Technical Note

DDR2-533 Memory Design Guide for Two-DIMM Unbuffered Systems

Overview

DDR2 memory busses vary depending on the intended market for the finished product. Some products must support four or more registered DIMMs, while some are point-to-point topologies. This document focuses on solutions requiring two unbuffered DIMMs operating at a data rate of 533 megabits per second (Mb/s) and is intended to assist board designers with the development and implementation of their products.

The document consists of two sections. The first section uses data gathered from a chipset and motherboard designed by Micron to provide a set of board-design rules. These rules are meant to be a starting point for a board design. The second section details the process of determining the portion of the total timing budget allotted to the board interconnect. The intent is that board designers will use the first section to develop a set of general rules and then, through simulation, verify the design in their particular environments.

Introduction

Systems using unbuffered DIMMs can implement the address and command bus using various configurations. For example, some controllers have two copies of the address and command bus, so the system can have one or two DIMMs per copy, but never more than two DIMMs total. Further, the address bus can be clocked using 1T or 2T clocking. With 1T, a new command can be issued on every clock cycle. 2T timing will hold the address and command bus valid for two clock cycles. This reduces the efficiency of the bus to one command per two clocks, but it doubles the amount of setup and hold time. The data bus remains the same for all of the variations in the address bus.

This design guide covers a DDR2 system using two unbuffered DIMMs, operating at a 533Mb/s data rate and two variations of the address and command bus. The first variation covered is a system with one DIMM per copy of the address and command bus using 1T clocking. A block diagram of this topology is shown in Figure 1 on page 2. The second variation is a system with two DIMMs on the address and command bus using 2T clocking topology, as shown in Figure 2 on page 3. Please note that the guidelines provided in this section are intended to provide a set of rules for board designers to follow, but it is always advisable to simulate the final implementation to ensure proper functionality.

Figure 1: Two-DIMM Unbuffered DDR2-533 MHz Topology 1T Address and Command Bus

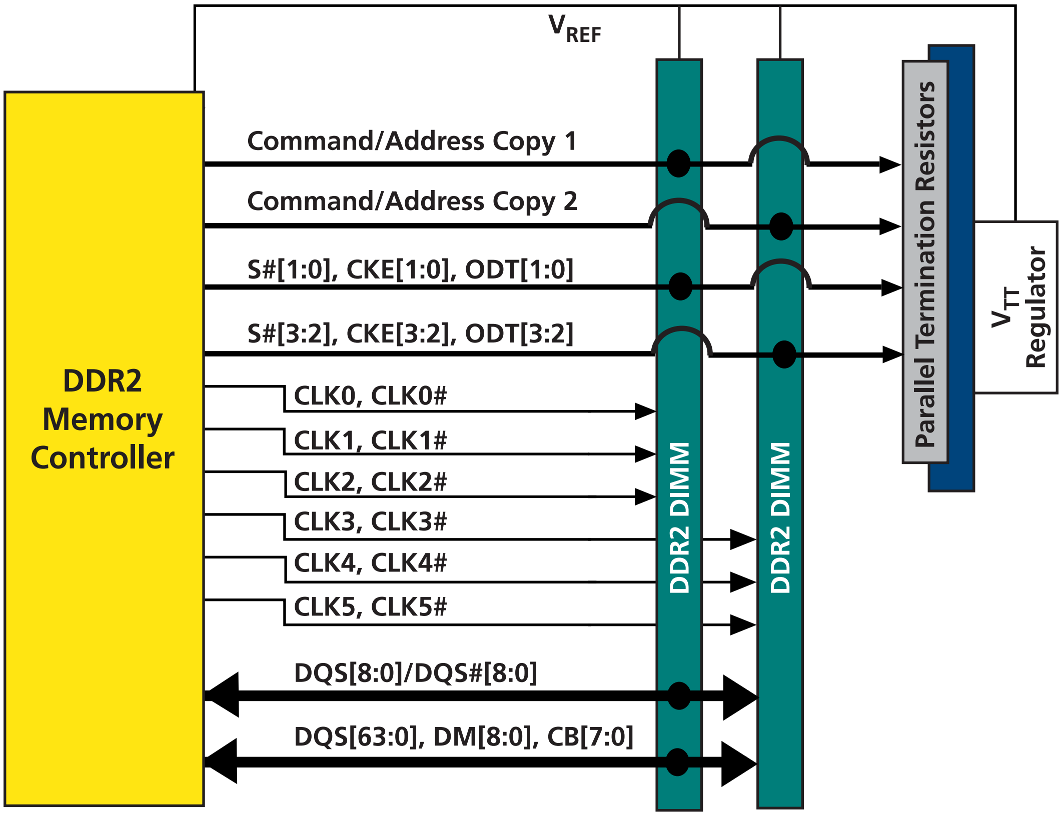
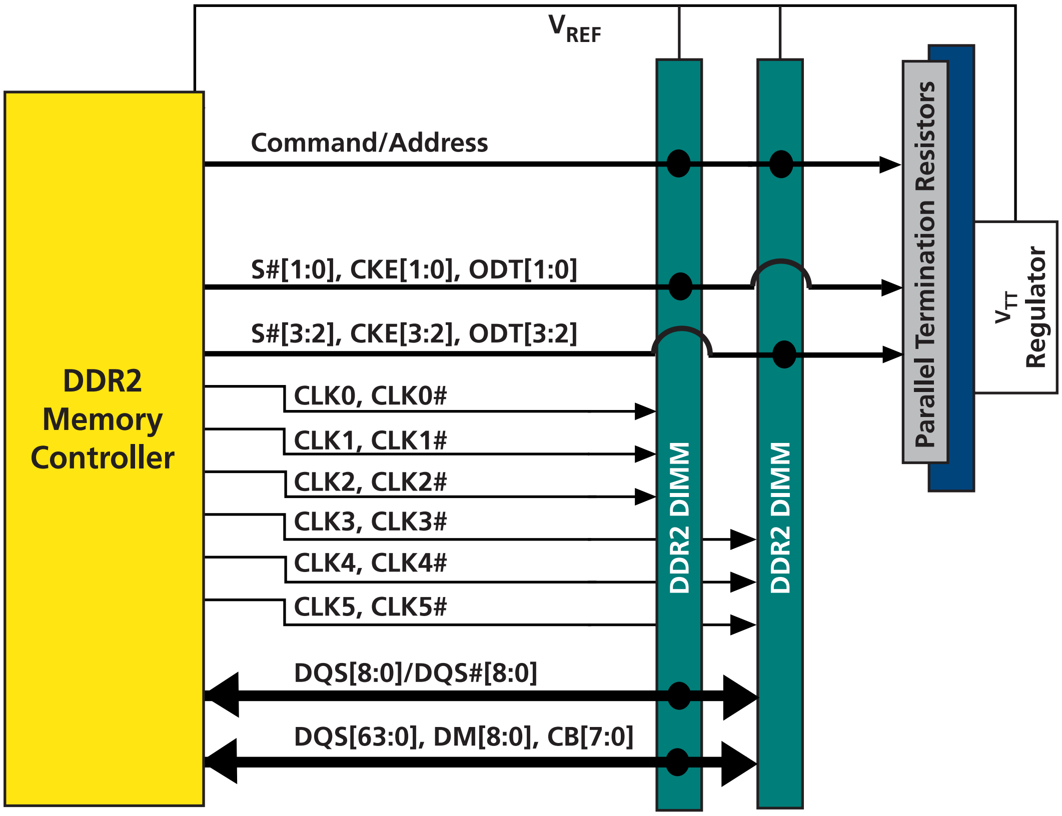


Figure 2: Two-DIMM Unbuffered DDR2-533 MHz Topology 2T Address and Command Bus



DDR2 Signal Grouping

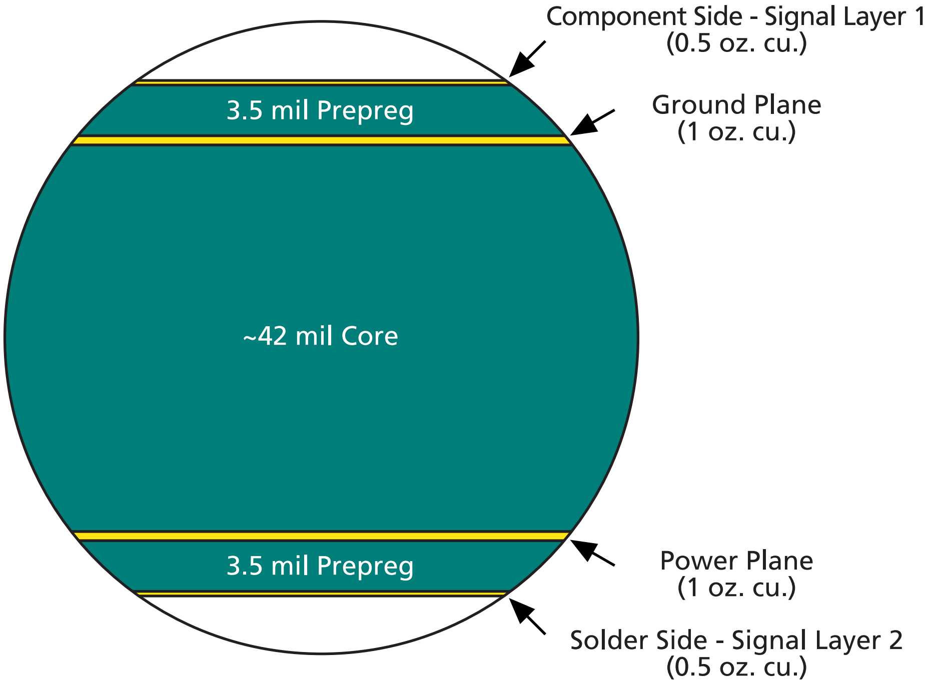
The signals that compose a DDR2 memory bus can be divided into four unique groupings, each with its own configuration and routing rules.

- **Data Group:** Data Strobe DQS[8:0], Data Strobe Complement DQS#[8:0](Optional), Data Mask DM[8:0], Data DQ[63:0], and Check Bits CB[7:0]
- **Address and Command Group:** Bank Address BA[2:0], Address A[15:0], and Command Inputs RAS#, CAS#, and WE#.
- **Control Group:** Chip Select S[3:0]#, Clock Enable CKE[3:0], and On-die Termination ODT[3:0]
- **Clock Group:** Differential Clocks CK[5:0] and CK#[5:0]

Board Stackup

A two-DIMM DDR2 channel can be routed on a four-layer board. The layout should be done using controlled impedance traces of Zo = 50Ω (±10%) characteristic impedance. A sample stackup is shown in Figure 3. The trace impedance is based on a 5-mil-wide trace and 1/2 oz. copper with a dielectric constant of 4.2 for the FR4 prepreg material. This stackup assumes that the 1/2 oz. copper on the outer layers is plated, for a total thickness of 2.1 mils. Other solutions exist for achiving a 50Ω characteristic impedance, so board designers should work with their PCB vendors to specify a stackup.

Figure 3: Sample Board Stackup



Address and Command Signals - 2T Clocking

On a DDR2 memory bus, the address and command signals are unidirectional signals driven by the memory controller. For DDR2-533 using 2T on the address and command signals, the address and command bus runs at a max switching rate of 133 MHz. The address and command signals are captured at the DRAM using the memory clocks. For a system with two unbuffered DIMMs on a single address and command bus, the loading on these signals will differ greatly depending on the type and number of DIMMs installed. A two-DIMM channel loaded with two double-sided DIMMs has 36 loads on the address and command signals. Under this heavy loading, the slew rate on the address bus is slow. The reduced slew rate makes it difficult, if not impossible, to meet the setup and hold times at the DRAM. To address this issue, the controller can use 2T address timing—increasing the time available for the address command bus by one clock period. Note that S#, ODT, and CKE timing does not change between 1T and 2T addressing.

2T Address and Command Routing Rules

It is important that the address and command lines be referenced to a solid V_{DD} power plane. V_{DD} is the 1.8V supply that also supplies power to the DRAM on the DIMM. On a four-layer board, the address and command would typically be routed on the second signal layer referenced to a solid power plane. The system address and command signals should be power referenced over the entire bus to provide a low-impedance current return path. The DDR2 Unbuffered DIMMs also reference the address and control signals to V_{DD} so the power reference is maintained onto the module. The address and command signals should be routed away from the data group signals, from the controller to the first DIMM. Address and command signals are captured at the DIMM using the clock signals, so they must maintain a length relationship to the clock signals at the DIMM.

Figure 4: DDR2 Address and Command Signal Group 2T Routing Topology

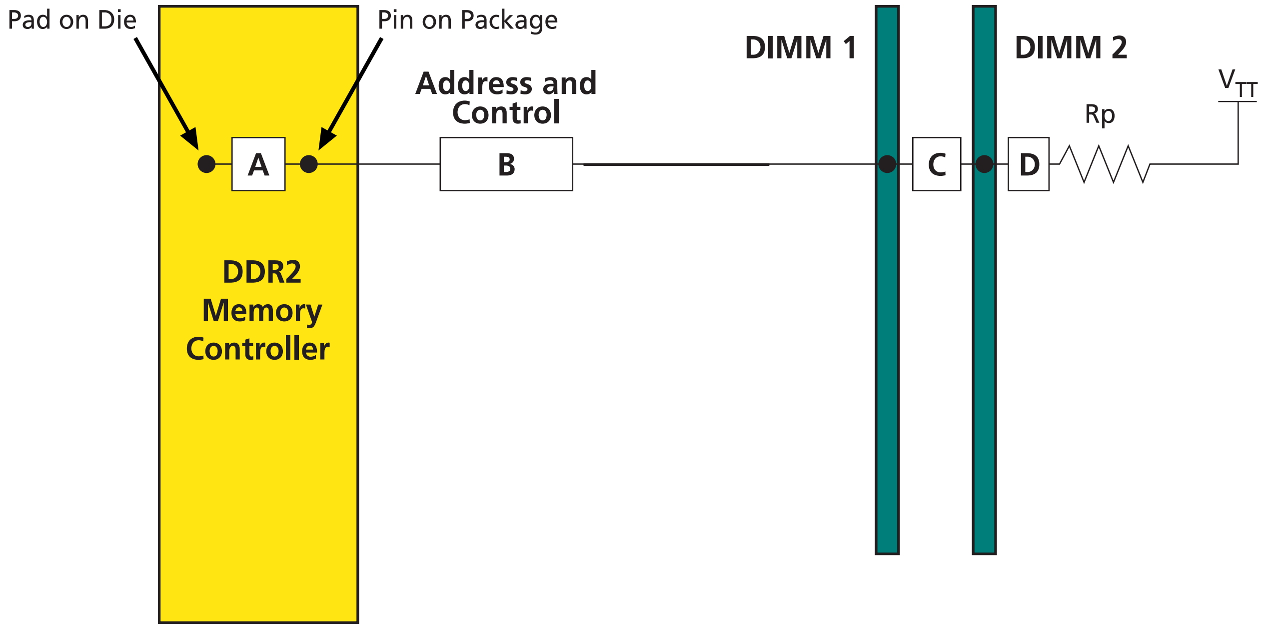


Table 1: Address and Command Group 2T Routing Rules

Length
A = Obtain from DRAM controller vendor. (A is the length from the die pad to the ball on the ASIC package.) B = 1.9in.–4.5in. C = 0.425in. D = 0.2in.–0.55in. **Total:** A + B + C = 2.5in.–5.0in.
Length Matching
+200 mils of memory clock length at the DIMM[1]
Trace
Trace width = 5 mils–target 50 or 60Ω impedance Trace space = 12–15 mils reducing to 11.5 mils going between the pins of the DIMM Trace space from DIMM pins = 7 mils Trace space to other signal groups = 20–25 mils

Notes: 1. This value is controller-dependent; see “Clock Signal Routing Rules” on page 16.

Parallel/Pull-up Resistor (Rp) Termination Resistor

- **Location:** The parallel termination resistors should be placed behind the last DIMM slot and attached to the V_{TT} power island.
- **Value:** The value of the parallel resistor can vary depending on the bus topology.
- **Range:** 36Ω–56Ω
- **Recommended:** 47Ω

Note: These are recommended values. A range of values is provided for simulation when there is a need to deviate from the recommendation.

Address and Command Signals - 1T Clocking

On a DDR2 memory bus, the address and command signals are unidirectional signals that are always driven by the memory controller. For DDR2-533, the address runs at a clock rate of 266 MHz. The address and command signals are captured at the DRAM using the memory clocks. For a system with two unbuffered DIMMs on a single address and command bus, the loading on these signals will differ greatly depending on the type and number of DIMMs installed. A two-DIMM channel loaded with two double-sided DIMMs has 36 loads on the address and command signals. The heavy capacitive load causes a significant reduction in signal slew rate and voltage margin at the DRAM. The reduced voltage margin causes a reduction in timing margin. As a result, setup and hold times at the DRAM may not be met.

To increase the timing margin, the loading on the address and command bus must be reduced. Some controllers will provide two copies of the address and command bus. One copy is connected to each DIMM, reducing the total maximum load on the bus to 18 loads. By reducing the maximum loading, the timing margin is increased to a point that 1T timing of the address bus is achievable. Figure 5 on page 7 shows a block diagram of the address and command bus for 1T timing.

The addition of an extra copy of address and command signals helps improve the signaling but the reduction in loading alone may not be enough to meet setup and hold times for 1T signals. The addition of a compensation capacitor to the address and command signals will further improve the signal quality. Figure 6 on page 8 shows the difference in signal quality between a system with the compensation capacitor and one without it. These simulation results clearly show the improvements in signal quality and as a result improved address valid window when the compensation capacitor is added to the address and command signals.

Figure 5: DDR2 Address and Command Signal Group 1T Routing Topology

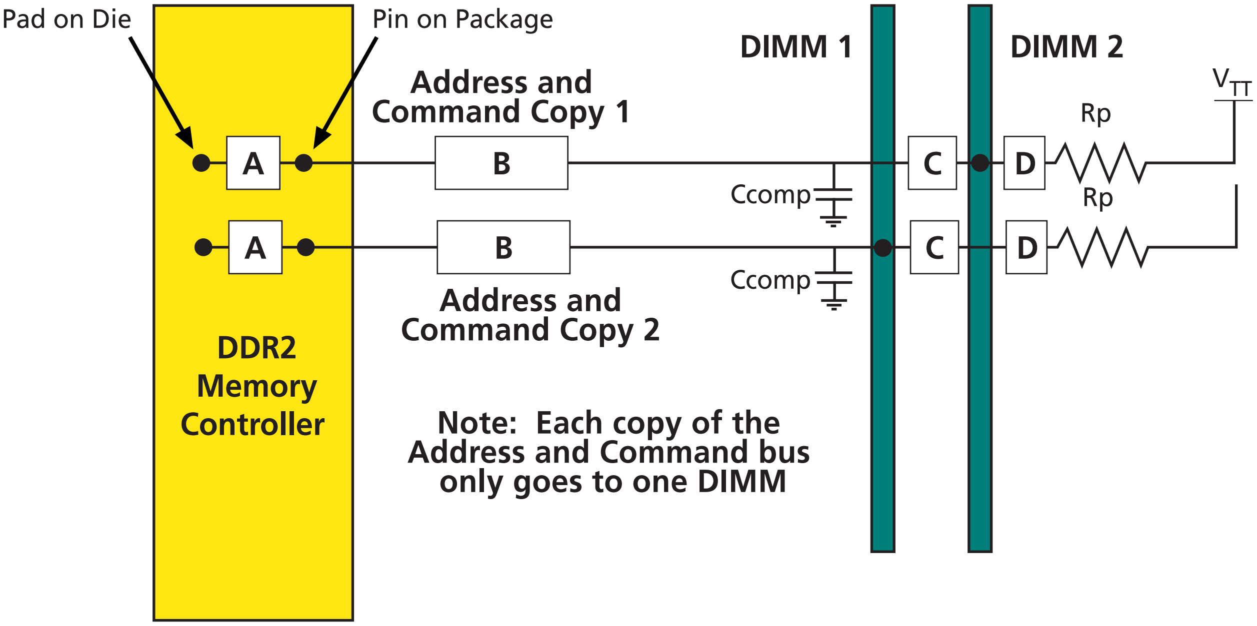


Figure 6: DDR2 Address Compensation Capacitor Signal Quality Improvements

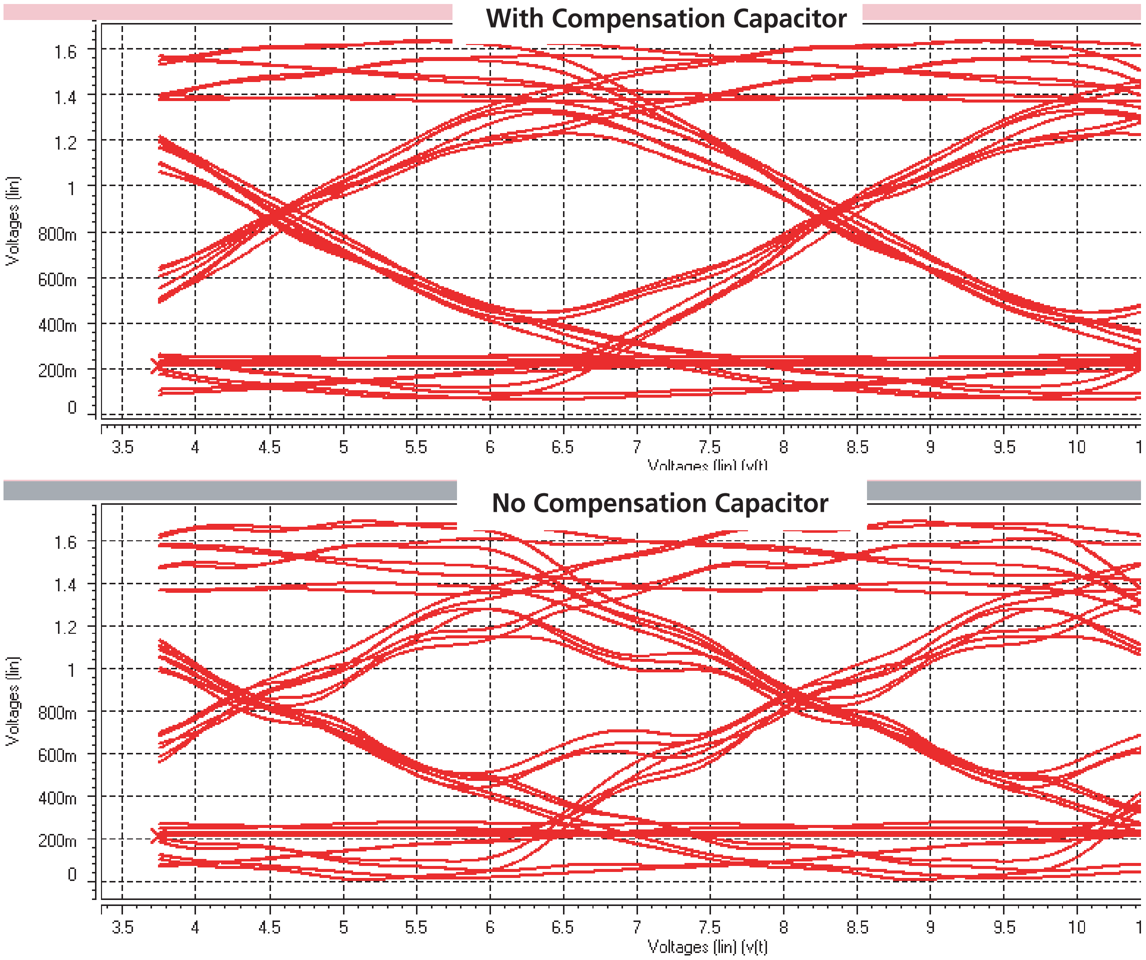


Table 2: Address and Command Group 1T Routing Rules

Length
A = Obtain from DRAM controller vendor. (A is the length from the die pad to the ball on the ASIC package.) B = 1.9in.–4.5in. C = 0.425in. D = 0.2in.–0.55in. **Total:** A + B + C = 2.5in.–5.0in.
Length Matching
+200 mils of memory clock length at the DIMM[1]
Trace
Trace width = 5 mils–target 50Ω impedance Trace space = 12–15 mils reducing to 11.5 mils going between the pins of the DIMM Trace space from DIMM pins = 7 mils Trace space to other signal groups = 20–25 mils

Notes: 1. This value is controller-dependent; see “Clock Signal Routing Rules” on page 16.

1T Address and Command Routing Rules

It is important that the address and command lines be referenced to a solid power or ground plane. On a four-layer board, the address and command would typically be routed on the second signal layer referenced to a solid power plane. The system address and command signals should be power-referenced over the entire bus to provide a low-impedance current-return path. The address and command signals should be kept from the data group signals, from the controller to the first DIMM. Address and command signals are captured at the DIMM using the clock signals, so they must maintain a length relationship to the clock signals at the DIMM.

Compensation Capacitor (Ccomp)

- **Location:** Ccomp is placed 0.5in. to 1.0in. from the first DIMM slot.
- **Value:** The value of Ccomp can vary depending on the bus topology.
- **Recommended:** 24pF
- **Range:** 18-27pF

Note: These are recommended values. A range of values is provided for simulation when there is a need to deviate from the recommendation.

Parallel/Pull-Up Resistor (Rp) Termination Resistor

- **Location:** The parallel termination resistors should be placed behind the last DIMM slot and attached to the V_{TT} power island.
- **Value:** The value of the parallel resistor can vary depending on the bus topology.
- **Range:** 36Ω–56Ω
- **Recommended:** 47Ω

Note: These are recommended values. A range of values is provided for simulation when there is a need to deviate from the recommendation.

Control Signals

The control signals in a DDR2 system differ from the address in two ways. First, the control signals must use 1T timing. Second, each DIMM rank has its own copy of the control signals. A new feature introduced with DDR2 is on-die termination (ODT) signals.

ODT signals are used to control the termination of the data group signals in the DDR2 DRAM device. DDR2 no longer uses the serial and parallel termination resistors on the data group signals that are used in DDR systems. DDR2 uses a new termination scheme, with the signals terminated in the DRAM device and the controller by internal termination resistors. ODT signals are used to enable or disable the termination in the DRAM depending on the type of bus transition and the system load. Table 3 on page 10 and Table 4 on page 10 show the termination values used for reads and writes. Figure 7 on page 11 shows a block diagram of the topology used for the control signals. A compensation capacitor is not required on the motherboard for the control signals. The compensation capacitor for the control signals has been placed on the unbuffered DIMMs.

Table 3: DDR2 ODT Control for Write Case

Configuration	Write to	Controller	Module 1	Module 2
1 slot populated	Slot 1	Infinite	150Ω	Empty
	Slot 2	Infinite	Empty	150Ω
2 slots populated	Slot 1	Infinite	Infinite	75Ω
	Slot 2	Infinite	75Ω	Infinite

Table 4: DDR2 ODT Control for Write Case

Configuration	Write to	Controller	Module 1	Module 2
1 slot populated	Slot 1	75Ω	Infinite	Empty
	Slot 2	75Ω	Empty	Infinite
2 slots populated	Slot 1	150Ω	Infinite	75Ω
	Slot 2	150Ω	75Ω	Infinite

Figure 7: DDR2 Control Signal Group Routing Topology

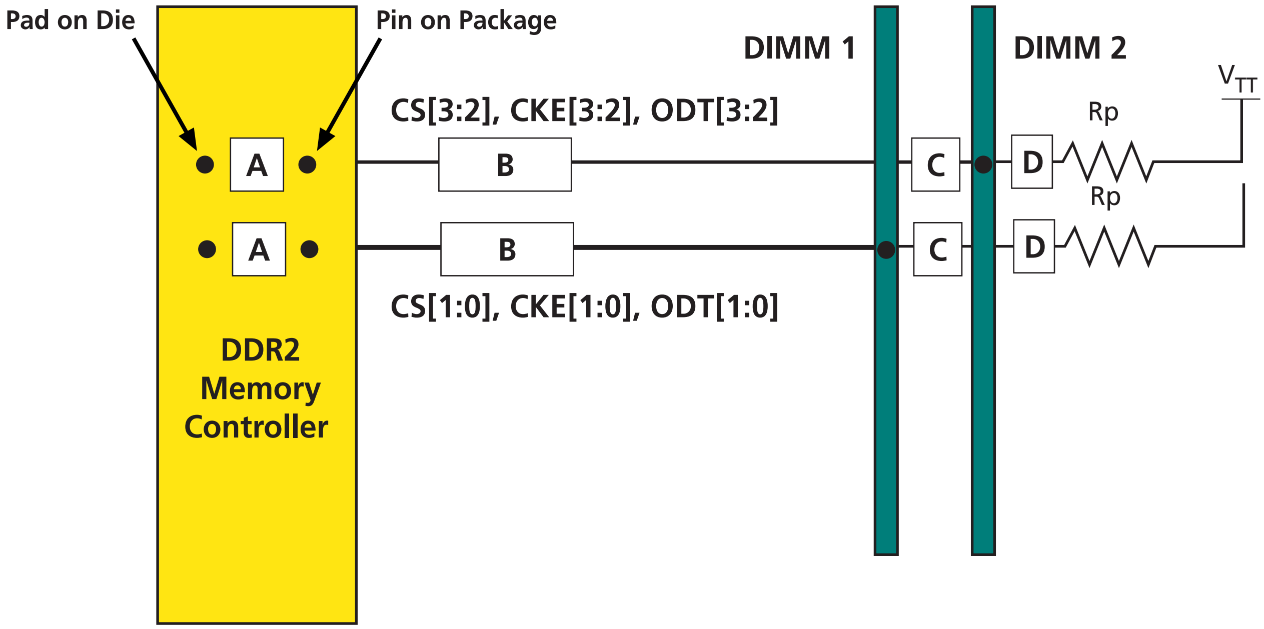


Table 5: Control Group Routing Rules

Length
A = Obtain from DRAM controller vendor. (A is the length from the die pad to the ball on the ASIC package.) B = 1.9in.–4.5in. C = 0.425in. D = 0.2in.–0.55in. **Total:** A + B + C = 2.5in.–6.0in.
Length Matching
+200 mils of memory clock length at the DIMM[1]
Trace
Trace width = 5 mils–target 50Ω impedance Trace space = 12–15 mils reducing to 11.5 mils going between the pins of the DIMM Trace space from DIMM pins = 7 mils Trace space to other signal groups = 20–25 mils

Notes: 1. This value is controller-dependent; see “Clock Signal Routing Rules” on page 16.

Control Signal Routing Rules

Like the address signals, the control signals must be referenced to a solid power or ground plane. On a four-layer board, the control signals would typically be routed on the second signal layer referenced to a solid power plane. The system control signals must be power-referenced over the entire bus to provide a low-impedance current-return path. Unlike the address signals, the control signals are routed point-to-point from the controller to the DIMM. The control signals do not require any series or parallel resistance. The control signals must be routed with clearance from the data group signals, from the controller to the first DIMM. Control signals are captured at the DIMM using the clock signals, so they must maintain a length relationship to the clock signals at the DIMM.

Parallel/Pull-Up Resistor (Rp) Termination Resistor

- **Location:** The parallel termination resistors should be placed behind the last DIMM slot and attached to the V_{TT} power island.
- **Value:** The value of the parallel resistor can vary depending on the bus topology.
- **Range:** 36Ω–56Ω
- **Recommended:** 47Ω

Note: These are recommended values. A range of values is provided for simulation when there is a need to deviate from the recommendation.

Data Signals

In a DDR2 system, the data is captured by the memory and the controller using the data strobe rather than the clock. DDR2 also has the option of having data strobe complement (DQS#) signals. If the data strobe complement signals are implemented, they must be routed as a differential pair with the data strobe. To achieve the double data rate, data is captured on the rising and falling edges of the data strobe (DQS) or each crossing point if using DQS/DQS# pairs. Each 8 bits of data has an associated data strobe (DQS), optional data strobe complement (DQS#), and a data mask bit (DM). Because the data is captured off the strobe, the data bits associated with the strobe must be length-matched closely to their strobe bit. This group of data and data strobe is referred to as a byte lane. The length-matching between byte lanes is not as tight as it is within the byte lane. Table 6 shows the data and data strobe byte lane groups. Figure 8 on page 15 shows the signals in a single-byte lane and the bus topology for the data signals.

Data Signal Routing Rules

It is important that the data lines be referenced to a solid ground plane. These high-speed data signals require a good ground-return path to avoid degradation of signal quality due to inductance in the signal-return path. The system data signals should be ground-referenced from the memory controller to the DIMM connectors and from DIMM connector to DIMM connector to provide a low-impedance current-return path.

This is accomplished by routing the data signals on the top layer for the entire length of the signal. The data signals should not have any vias.

Table 6: Data to Data Strobe Grouping

Data	Data Strobe	Data Strobe Complement	Data Mask
DQ[7:0]	DQS 0	DQS# 0	DM 0
DQ[15:8]	DQS 1	DQS# 1	DM 1
DQ[23:16]	DQS 2	DQS# 2	DM 2
DQ[31:24]	DQS 3	DQS# 3	DM 3
DQ[39:32]	DQS 4	DQS# 4	DM 4
DQ[47:40]	DQS 5	DQS# 5	DM 5
DQ[55:48]	DQS 6	DQS# 6	DM 6
DQ[63:56]	DQS 7	DQS# 7	DM 7
CB[7:0]	DQS 8	DQS# 8	DM 8

Table 7: Data Group Routing Rules

Length
A = Obtain from DRAM controller vendor. (A is the length from the die pad to the ball on the ASIC package.) B = 1.9in.–4.5in. C = 0.425in. D = 0.2in.–0.55in. **Total:** A + B + C = 2.5in.–5.0in.
Length Matching in Data/Strobe Byte Lane
+50 mils from data strobe[1]
Length Matching Byte Lane to Byte Lane
±0.5in. of memory clock length
Trace
Data: Trace width = 5 mils–target 50Ω impedance Trace space = 12–15 mils reducing to 11.5 mils going between the pins of the DIMM Trace space from DIMM pins = 7 mils Trace space to other signal groups = 20–25 mils **Differential strobe:** Trace width = 5 mils–target 50Ω impedance Trace space = 5 mils between pairs Trace space to other signals = 25 mils

Notes: 1. This value assumes differential strobes are used. Differential signals have a faster propagation time than single-ended signals, so if the data signals are routed equal to or longer than the data strobe, the data strobe signal will arrive at the DRAM in the center of its associated data signals. The propagation delay can vary with design parameters, so simulation of these signals is recommended.

Clock Signals

The memory clocks CK[5:0] and CK#[5:0] are used by the DRAM on a DDR2 bus to capture the address and command data. Unbuffered DIMMs require three clock pairs per DIMM. Some DDR2 memory controllers will drive all of these clocks, while others will require an external clock driver to generate these signals. In this example, it is assumed that the memory controller will drive the six clock pairs required for a two-DIMM unbuffered system.

Clocks do not get connected to V_{TT} like the address signals of a DDR2 bus. The clocks are differential pairs and must be routed as a differential pair. Each clock pair is differentially terminated on the DIMM. Figure 9 on page 16 shows the routing topology used for the clocks. In this figure, only one of the three clock pairs required by each DIMM is shown.

Figure 9 on page 16 also shows a capacitor placed between the clock pairs. This capacitor can improve the clock slew rates and signal quality at the DRAM. The ability of the capacitor to improve the clock signals is dependent on the clock driver. Some drivers will benefit from the addition of the capacitor more than others. Designers should check with their chipset provider to see if having a capacitor on the clocks is beneficial. If the capacitor is implemented, place it 0.5in. away from the first DIMM connector. The best value for the capacitor is 5pF.

Figure 8: DDR2 Data Byte Lane Routing Topology

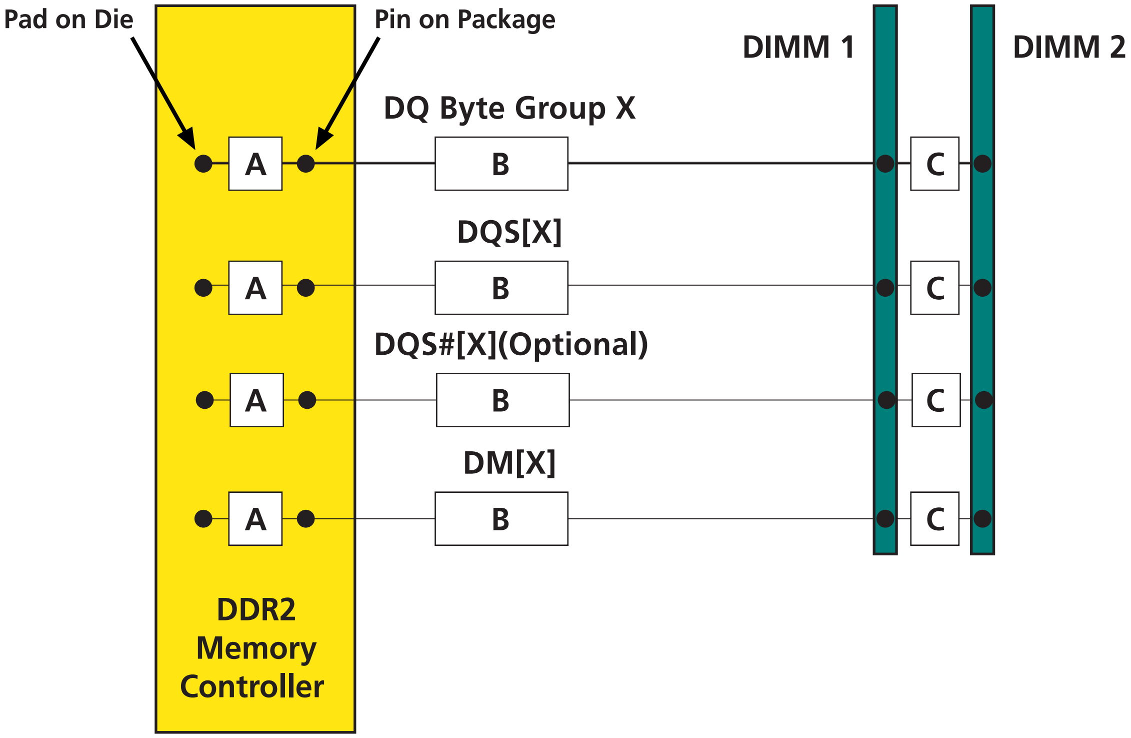
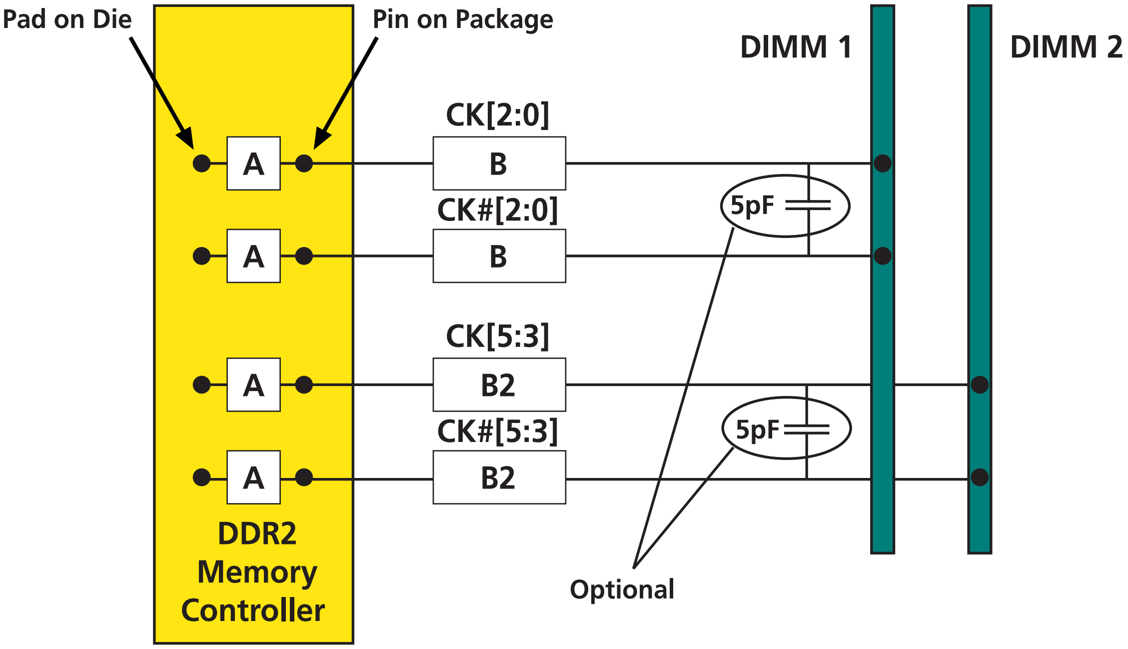


Figure 9: DDR2 Clock Signal Group Routing Topology



Clock Signal Routing Rules

The clocks are routed as a differential pair from the controller to the DIMM. The clocks are used to capture the address and control signals at the DRAM on the DIMM, so they must maintain a length relationship to the address and control signals at the DIMM to which they are connected. Most controllers have the ability to prelaunch the address and control signals. The prelaunch is used to center the clock in the address valid eye. It is required because the clocks are loaded lighter than the address signals and as a result have a shorter flight time from the controller to the DRAM on the DIMM. Differentially routed signals like the clock also have a shorter flight time than single-ended signals. This effect causes the clock signals to arrive at the DRAM even sooner than the address, command, and control signals. To compensate for the difference in propagating delay, it is recommended that the clock signals be roughly equal to or shorter than the address, command, and control signals.

Table 8: Clock Group Routing Rules

Length
A = Obtain from DRAM controller vendor. (A is the length from the die pad to the ball on the ASIC package.) B = 1.9in.–5.0in. B2= 2.325in.–5.425in.
Length Matching
±10 mils for CK to CK# ±25 mils clock pair to clock pair at the DIMM
Trace
Trace width = 8 mils–target 40Ω trace impedance, 70Ω differential impedance Trace space = 5 mils Trace space to other signal groups = 20 mils

DDR2 Memory Power Supply Requirements

A DDR2 bus implementation requires three separate power supplies. The DRAM and the memory portion of the controller require a 1.8-volt supply. The 1.8 volt supply provides power for the DRAM core and I/O as well as at least the I/O of the DRAM controller. The second power supply is V_{REF}, which is used as a reference voltage by the DRAM and the controller. The third supply is V_{TT}, which is the termination supply of the bus. Table 9 on page 19 lists the tolerances of each of these supplies.

MV_{TT} Voltage

The memory termination voltage, MV_{TT}, requires current at a voltage level of 900 mV(DC). See Figure 7 on page 11 for the V_{TT} tolerance. V_{TT} must be generated by a regulator that is able to sink and source current while still maintaining the tight voltage regulation.

- V_{REF} and V_{TT} must track variations in V_{DD} over voltage, temperature, and noise ranges.
- V_{TT} of the transmitting device must track V_{REF} of the receiving device.

MV_{TT} Layout Recommendations

- Place the MV_{TT} island on the component-side signals layer at the end of the bus behind the last DIMM slot.
- Use a wide-island trace for current capacity.
- Place the V_{TT} generator as close to the termination resistors as possible to minimize impedance (inductance).
- Place one or two 0.1µf decoupling caps by each termination RPACK on the MV_{TT} island to minimize the noise on V_{TT}. Other bulk (10µf–22µf) decoupling is also recommended to be placed on the MV_{TT} island.

MV_{REF} Voltage

The memory reference voltage, MV_{REF}, requires a voltage level of one-half V_{DD} with a tolerance as shown in Table 9. V_{REF} can be generated using a simple resistor divider with 1% or better accuracy. V_{REF} must track one-half of V_{DD} over voltage, noise, and temperature changes.

- Peak-to-peak AC noise on V_{REF} may not exceed ±2% $V_{REF(DC)}$.

MV_{REF} Layout Recommendations

- Use 30 mil trace between decoupling cap and destination.
- Maintain a 25 mil clearance from other nets.
- Simplify implementation by routing V_{REF} on the top signal trace layer.
- Isolate V_{REF} and/or shield with ground.
- Decouple using distributed 0.01µf and 0.1µf capacitors by the regulator, controller, and DIMM slots. Place one 0.01µf and 0.1µf near the V_{REF} PIN of each DIMM. Place one 0.1µf near the source of V_{REF}, one near the V_{REF} pin on the controller, and two between the controller and the first DIMM.

Table 9: Required Voltages

Symbol	Parameter	MIN	Typical	MAX	Unit
V_{DD}	Device supply voltage	1.7	1.8	1.9	V
V_{REF}	Memory reference voltage	V_{DD} * 0.49	V_{DD} * 0.5	V_{DD} * 0.51	V
V_{TT}	Memory termination voltage	V_{REF} - 40mV	V_{REF}	V_{REF} + 40mV	V

Timing Budget

The previous section is useful for getting an idea of how the DDR2 memory bus functions and the general relationship between the signals on the bus. However, if a design should deviate from the given example, the routing rules for the design can change. Since it is unlikely that every design will follow the given example exactly, it is important to simulate the design. One of the objectives of simulation is to determine if the design will meet the signal timing requirements of the DRAM and DDR2 controller. To meet this objective, a timing budget must be generated. This section shows how to use the data provided in the DDR2 DRAM and DDR2 controller data sheets to determine the amount of the total timing budget that the board interconnect can consume.

DDR2 Data Write Budget

Table 10 on page 20 gives specifics of the timing budget for DDR2 WRITEs at 533 MT/s. The portion of the budget consumed by the DRAM device and by the DDR2 controller is fixed and cannot be influenced by the board designer. The amount of the total budget remaining after subtracting the portion consumed by the DRAM and the controller is what remains for the board interconnect. This is the portion that is used to determine the bus routing rules. The different components of the board interconnect are outlined. The board designer can make trade-offs with trace spacing, length matching, resistor tolerance, etc., to determine the best interconnect solution.

Table 10: DDR2 Write Budget[1]

Element	Skew Component	Setup	Hold	Units	Comments
Transmitter	Total skew at transmitter	325	325	ps	From data sheet
Clock	Data/strobe PLL jitter	25	25	ps	May be included in transmitter setup and hold
DRAM device (from spec)	$^tDH/^tDS$	100	225	ps	
	Total device	350	350	ps	From data sheet
Interconnect	XTK (cross talk) - DQ	55	55	ps	4 aggressors (a pair on each side of the victim); victim (1010); aggressors (PRBS)
	XTK (cross talk) - DQS	40	40	ps	1 shielded victim, 2 aggressors (PRBS)
	ISI - DQ	30	30	ps	PBRS
	ISI - DQS	5	5	ps	1010...
	Input capacitance matching	25	25	ps	3.5pF and 4.0pF loads, strobe and data shift differently
	R_{EFF} mismatch	10	10	ps	+/- 3.75%
	Input eye reduction (V_{REF})	25	25	ps	±20mV included in DRAM skew; additional = (±25mV)/(1.0 V/ns); this includes DQ and DQS
	Path matching (board)	25	25	ps	Within byte lane: 165 ps/in. × 0.1in.; impedance mismatch within DQ to DQS
	Path matching (module)	10	10	ps	Module routing skew
Total interconnect	Interconnect skew	225	225	ps	
Total budget	1875/2 @ 533 MHz	937.5	937.5	ps	
Total budget consumed by controller and DRAM	Transmitter + DRAM + Interconnect	925	925	ps	
Interconnect budget	Total - (transmitter + DRAM + interconnect)	12.5	12.5	ps	Must be greater than 0

Notes: 1. These are worst-case slow numbers (85°C, 1.7V, slow process).

Determining DRAM Write Budget Consumption

The amount of the write budget consumed by the DRAM is easily obtained from the data sheets. The DRAM data sheet provides the data input hold time relative to strobe (^{t}DH) and the data input setup time relative to strobe (^{t}DS). These numbers are entered directly into the timing budgets for setup and hold. They account for all of the write timing budget consumed by the DRAM.

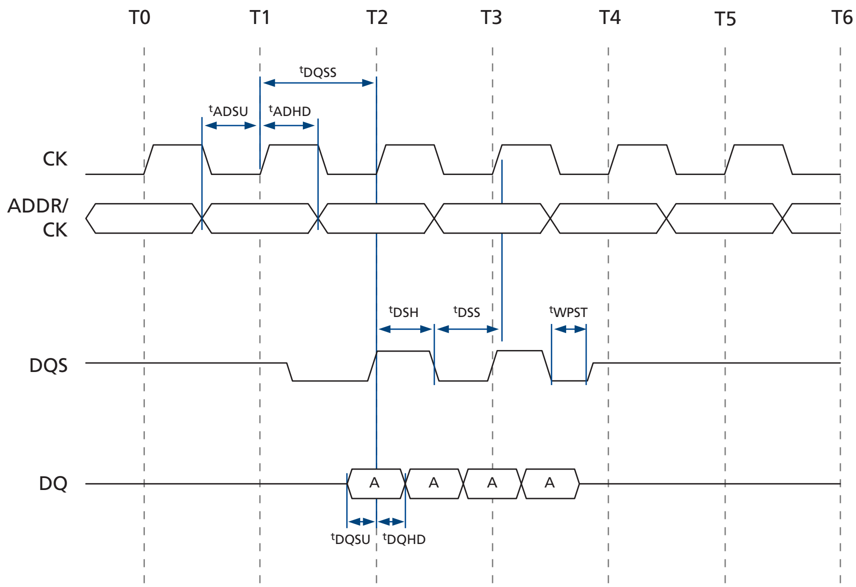
Determining DDR2 Controller Write Budget Consumption

To calculate the amount of the setup timing budget consumed by the DDR2 controller on a DRAM WRITE, find the value for ^{t}DQSU minimum. This is the minimum amount of time all data will be valid before the data strobe transitions shown in Figure 10. ^{t}DQSU should take clock asymmetry into account. In an ideal situation, ^{t}DQSU would be equal to 1/4 × ^{t}CK. The difference between 1/4 × ^{t}CK and ^{t}DQSU is the amount of the write timing budget consumed by the controller for setup. From this, the following equation is derived:

Controller setup data valid reduction = $1/4 \times {}^{t}\text{CK} - {}^{t}\text{DQSU}$

To calculate the hold time, use the same equation, but use ^{t}DQHD in place of ^{t}DQSU.

Figure 10: Memory Write and ADDR/CMD Timing



DDR2 Data Read Budget

Table 11 gives specifics of the timing budget for DDR2 reads at 533 MT/s. The portion of the budget consumed by the DRAM device and by the DDR2 controller is fixed and cannot be influenced by the board designer. The amount of the total budget remaining after subtracting the portion consumed by the DRAM and the controller is what remains for the board interconnect.

Table 11: DDR2 Read Budget[1]

Element	Skew Component	Setup	Hold	Units	Comments
DRAM device (from spec)	Clock ^{t}CK	3.75		ns	533 MT/s data rate
	^{t}HP (^{t}CL/^{t}CH[MIN] at 47/53)	1.763		ns	+/- 3% clock duty cycle
	^{t}DQSQ	300		ps	
	^{t}QHS	400		ps	
	^{t}QH (^{t}HP - ^{t}QHS)	1.363		ns	
	^{t}DV (^{t}HP - ^{t}DQSQ - ^{t}QHS, or ^{t}QH - ^{t}DQSQ)	1.063		ns	
	(^{t}CK/2 - ^{t}DV)/2	406	406	ps	
DRAM total	Total DRAM data valid reduction	406	406	ps	From data sheet.
Receiver (controller)	Total skew at receiver	275	275	ps	From data sheet
Clock	Data/strobe chip PLL jitter	25	25	ps	DRAM tester includes 50pS jitter margin
Interconnect	XTK (cross talk) - DQ	70	70	ps	Aggressors (a pair on each side of the victim); victim (1010); aggressors (PRBS)
	XTK (cross talk) - DQS	40	40	ps	1 shielded victim, 2 aggressors (PRBS)
	ISI - DQ	20	20	ps	Spice-generated eye diagram
	ISI - DQS	5	5	ps	1010...
	Path matching (board)	25	25	ps	Within byte lane: 165 ps/in. × 0.1in.; impedance mismatch within DQ to DQS
	Path matching (module)	10	10	ps	Module routing skew
	R_{EFF} mismatch	10	10	ps	+/- 3.75%
	Input eye reduction (V_{REF})	25	25	ps	±20mV included in DRAM skew; additional = (±25mV)/(1.0 V/ns); this includes DQ and DQS
	Capacitive mismatch	10	10		Capacitive load differences at the receiver in a byte
Total interconnect	Total skew at interconnect	215	215	ps	From simulation
Total budget	1875/2 @ 533 MHz	937.5	937.5	ps	
Total budget consumed by controller, DRAM, and interconnect	Receiver + DRAM + Interconnect	921	921	ps	
Interconnect budget	Total - (receiver + DRAM + interconnect)	16.5	16.5	ps	Must be greater than 0

Notes: 1. These are worst-case slow numbers (85°C, 1.7V, slow process).

Figure 11: DRAM Read Data Valid

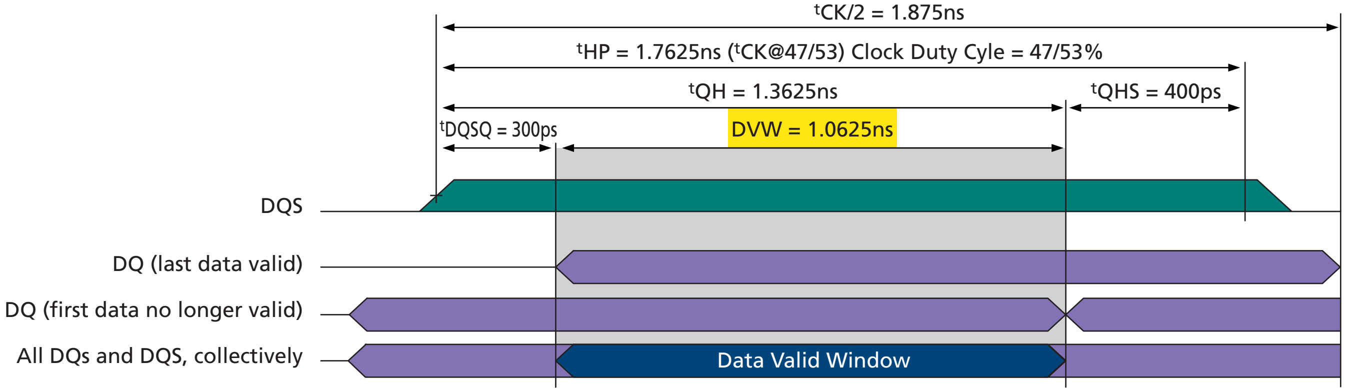
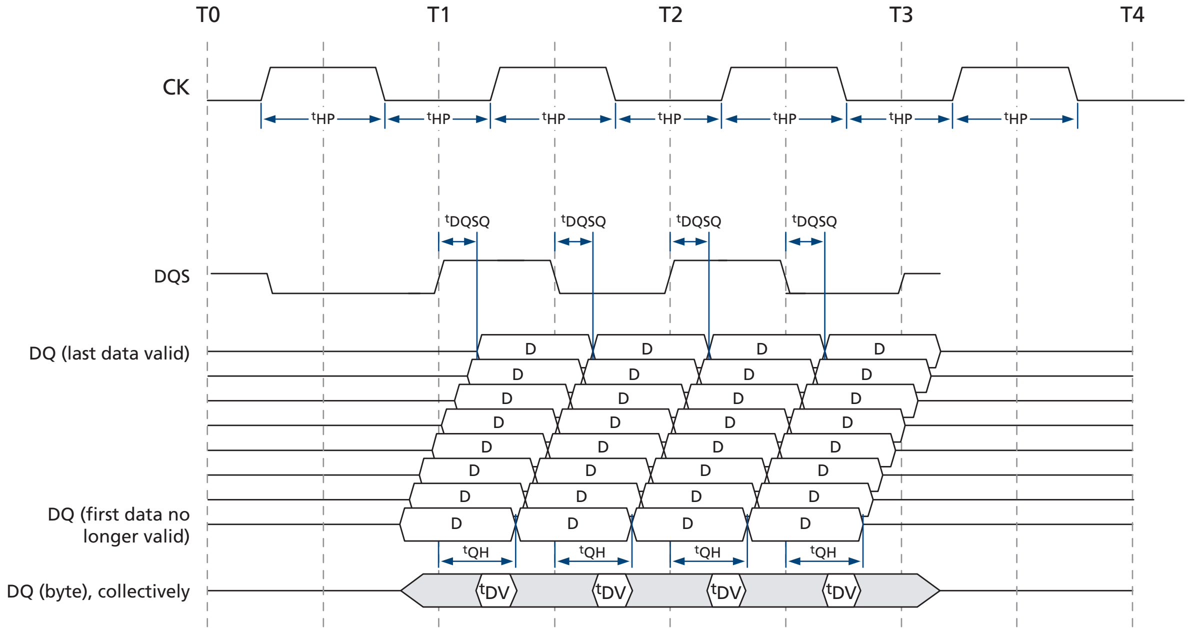


Figure 12: Read Data Timing



Determining DRAM Read Budget Consumption

Figure 11 shows how the information from the DRAM data sheet affects the total data valid window as the data is driven from the DRAM device. This information is used in the timing budget to determine the amount of the total data timing budget that is consumed by the DRAM device. The total budget for the data is half the clock period. This time is halved again to determine the time allowed for setup and hold. Using the DRAM data sheet and filling in numbers for the timing parameters in Figure 11, the total data valid window at the DRAM can be calculated using the following equation:

$$\text{DVW} = {}^{t}\text{HP} - {}^{t}\text{DQSQ} - {}^{t}\text{QHS}$$

$${}^{t}\text{CK}/2 - \text{DVW}/2 = \text{DRAM data valid reduction}$$

The DRAM data valid reduction is used in the timing budget for setup and hold.

Determining DDR2 Controller Read Budget Consumption

When read data is received at the controller from the DRAM, the strobe is edge-aligned with the data. It is the responsibility of the controller to delay the strobe and then use the delayed strobe to capture the read data. The controller will have a minimum value it can accept for a data valid window. Internally, the controller has a minimum setup and hold time that the data must maintain from the internally delayed strobe. Half the data valid window is the setup or hold time required by the controller plus any controller-introduced signal skew and strobe centering uncertainty. The timing diagram example in Figure 12 on page 23 shows the timing parameters required for calculating the data valid window. ^{t}DQSQ is the maximum delay from the last data signal to go valid after the strobe transitions. ^{t}QH is the minimum time all data must remain valid after strobe transitions. Use the following equation to obtain ^{t}DV:

$${}^{t}\text{DV} = {}^{t}\text{QH} - {}^{t}\text{DQSQ}$$

Assuming ^{t}DV is split evenly between setup and hold, the portion of the timing budget consumed by the controller for setup and hold is one-half ^{t}DV. For the controller used in this example, an even split between setup and hold can be assumed because the controller is determining the center of the data eye during the boot up routine, and the DLL maintains this relationship over temperature and voltage variations.

2T Address Timing Budget

Table 12 on page 25 gives specifics of the timing budget for a 2T address and command at a 266 MHz clock rate. Running the address and command at T2 with a 266 MHz clock results in a address frequency of 67 Mhz. The portion of the budget consumed by the DRAM device and the DDR2 controller is fixed and cannot be influenced by the board designer. The amount of the total budget remaining after subtracting the portion consumed by the DRAM and the controller is what remains for the board interconnect.

Determining DRAM Address Budget Consumption

The portion of the address budget consumed by the DRAM is obtained by getting the value of ^{t}IS for setup and ^{t}IH for hold. ^{t}IH and ^{t}IS are the setup and hold times required by the DRAM inputs. For systems with heavy loading on the address and command lines, the value in the data sheet must be derated depending on the slew rate. See the DRAM data sheet for information about derating.

Determining Controller Address Budget Consumption

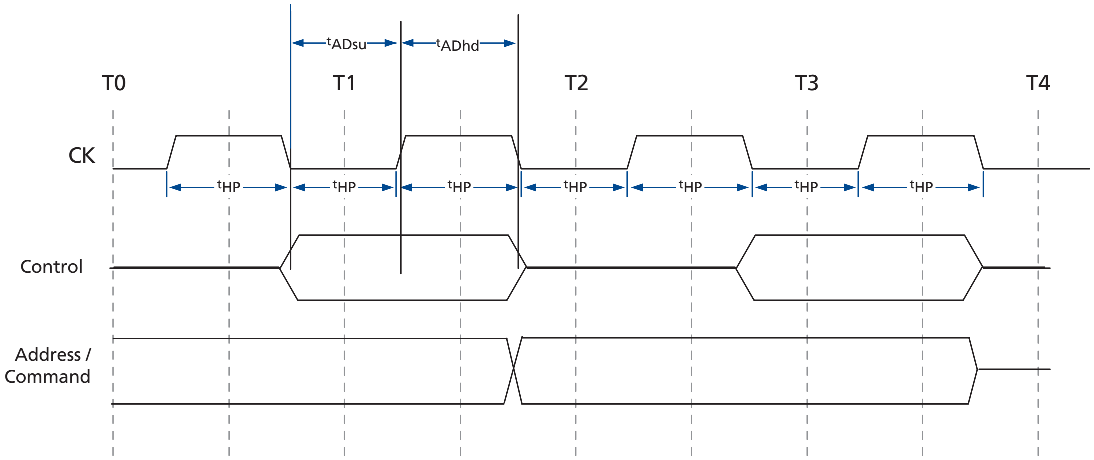
The DRAM controller will provide a minimum setup and hold time for the address and command signals with respect to clock. This is the amount of the setup and hold budget consumed by the controller.

Table 12: 2T Address Timing Budget[1]

Element	Skew Component	Setup	Hold	Units	Comments
Transmitter	Memory controller transmitter	550	550	ps	Chipset
Receiver	DRAM skew	250	375	ps	^{t}IS, ^{t}IH from DRAM spec (0.3V/ns to 1V/ns) (see derating table if outside this range)
Interconnect	Cross talk: address	250	250	ps	1 victim (1010...), 4 aggressors (PRBS)
	ISI: address	335	335	ps	(PRBS)
	Cross talk: clock	25	25	ps	Spec
	V_{REF}: reduction	100	100	ps	±75mV included in DRAM skew; additional = (±30mV)/(0.3 V/ns)
	Path matching	25	25	ps	Within byte lane: 165 ps/in. × 0.15in.; MB routes account for MC package skew
	DIMM config/loading mismatch	370	370	ps	Config: DIMM0/DIMM1 = 5/18 vs. 18/18 vs. 5/0.
	Rterm V_{OH}/V_{OL} skew (5%)	25	25	ps	Estimator tool (slew = 0.3V/ns, Rp = 47, V_{OUT} = 1.63V)
Total interconnect	Total skew at interconnect	1130	1130	ps	
Total budget	7500 @ 133 MHz	3750	3750	ps	133 MHz bit width
Total budget consumed by controller and DRAM	Transmitter + DRAM + interconnect	1930	2055	ps	
Interconnect budget	Total - (transmitter + DRAM)	1820	1695	ps	Must be greater than 0.

Notes: 1. These are worst-case slow numbers (85°C, 1.7V, slow process).

Figure 13: Control and 2T Address Timing



Control Signal Timing Budget

The control signals always operate with 1T timing, regardless of the address signals using 1T or 2T. Even when using 2T on the address signals, careful attention to the control signals is required. As shown in the timing diagram in Figure 13 on page 26, the control signals will have half the time of the 2T address signals to meet setup and hold times. Because the loading on the control signals is much less than the address signals, the task of closing timing is possible.

The timing budget for the control signals is derived in the same manner as the address signals. The only difference is the amount of time per cycle. For a 266 MHz clock frequency, the control signal period is 3.75ns. Table 13 on page 28 shows the timing budget for the control signals. Two items stand out as being very different from the address timing budget. First, the portion of the budget consumed by the DRAM is reduced for the control signals. The reduced loading on the control signals results in increased edge rates. The edge rates are fast enough that derating of the setup and hold time is not required. Second, the portion on the timing budget consumed by variation in the DIMM configuration and loading conditions is greatly reduced. Each rank in the system has its own copy of the control signals, so the loading on these signals is not affected by changes in total system loading in the same way as the address bus. These two differences make the task of closing the control signal timing budget possible.

In the timing of all the signal groups in a system, the control signals valid eye falls within the 2T address valid eye. Figure 14 shows a timing diagram that illustrates the timing relationships. The address signals have a longer transitioning time due to the slower slew rates. This relationship will hold true so long as the address signals and the control signals are held to the same setup and hold timing rules. So long as this relationship holds true, a closed 1T control timing budget will result in a closed 2T address budget. To make this relationship remain true, system designers must subject all control, address, and command signals to the same length-matching rules. When designing the relationship of the clock to the control, address, and command signals, it must be centered with respect to the 1T signals. This is accomplished with controller prelaunch and/or board routing.

Figure 14: Control, Address, and Command Timing Relationship

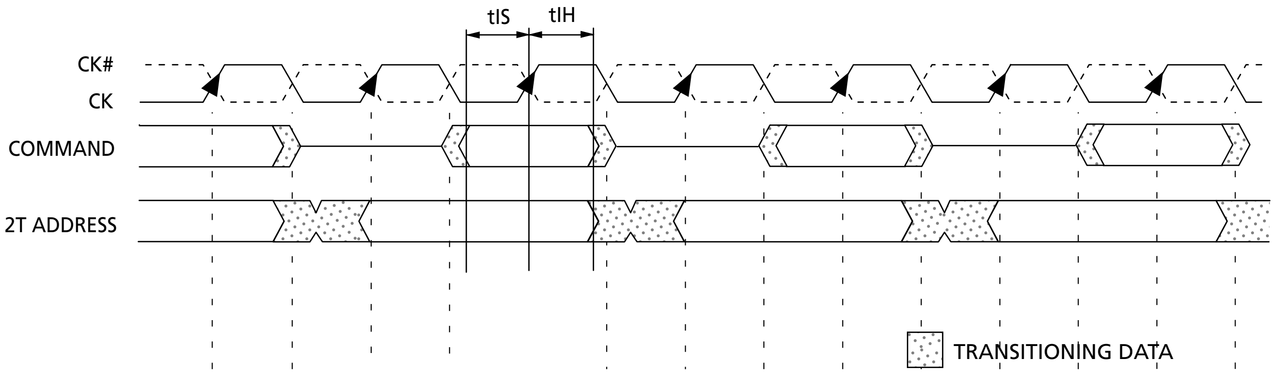


Table 13: Control Signals Timing Budget[1]

Element	Skew Component	Setup	Hold	Units	Comments
Transmitter	Memory controller transmitter	550	550	ps	Chipset
Receiver	DRAM skew	250	375	ps	^{t}IS, ^{t}IH from DRAM spec (0.3V/ns to 1V/ns) (see derating table if outside this range)
Interconnect	Cross talk: address	250	250	ps	1 victim (1010...), 4 aggressors (PRBS)
	ISI: address	325	325	ps	(PRBS)
	Cross talk: clock	50	50	ps	Spec.
	V_{REF}: reduction	50	50	ps	±75mV included in DRAM skew; additional = (±30mV)/(0.3 V/ns)
	Path matching	25	25	ps	Within byte lane: 165 ps/in. × 0.15in.; MB routes account for MC package skew
	DIMM config/loading mismatch	50	50	ps	Config: DIMM0/DIMM1 = 5/18 vs. 18/18 vs. 5/0
	Rterm V_{OH}/V_{OL} skew (5%)	15	15	ps	Estimator tool (slew = 0.3V/ns, Rp=47, V_{OUT}=1.63V)
Total interconnect	Total skew at interconnect	765	765	ps	
Total budget	3750 @ 266 MHz	1875	1875	ps	266 MHz bit width
Total budget consumed by controller and DRAM	Transmitter + DRAM + interconnect	1565	1690	ps	
Interconnect budget	Total - (transmitter + DRAM + interconnect)	310	185	ps	Must be greater than 0

Notes: 1. These are worst-case slow numbers (85°C, 1.7V, slow process).

Clock to Data Strobe Relationship

The DDR2 DRAM and the DDR2 controller must move the data from the data strobe clocking domain into the DDR2 clock domain when the data is latched internally. Due to this requirement, the data strobe must maintain a relationship to the DDR2 clock. For the DDR2 DRAM, this relationship is specified by ^{t}DQSS. This timing parameter states that after a WRITE command, the data strobe must transition 0.75 to 1.25 × ^{t}CK. Figure 10 on page 21 shows the DDR2 controller also specifies a ^{t}DQSS timing parameter. This is the time after the WRITE command that the data strobe will transition. For the controller in this example, $^t\text{DQSS} = \pm 0.06 \times {}^t\text{CK}$. The following equation is used to calculate the amount of clock to data strobe skew that is left for consumption by the board interconnect:

$$\text{Interconnect budget} = \text{DRAM } {}^t\text{DQSS} - \text{Controller } {}^t\text{DQSS}$$

This equation shows that clock to data strobe is not one of the strict timing requirements of a DDR2 channel. If the clocks are routed so that they are between the shortest and longest strobe lengths, designers gain some leeway in the data strobe to data strobe byte lane routing restrictions.

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