Schematic Review Checklist for Numonyx™ StrataFlash® Wireless Memory (L18/L30) and Numonyx™ Wireless Flash Memory (W18/W30)

Application Note - 783

November 2007

253165-02

Contents

Contents

Date of Revision	Version	Description
05/30/03	-001	Initial Release
November 2007	02	Applied Numonyx branding.

1.0 Introduction

This document provides hardware design information for system designers using the Numonyx™ StrataFlash® Wireless Memory (L18/L30) and the Numonyx™ Wireless Flash Memory (W18/W30) devices. This document is intended as a checklist for designers conducting schematic design reviews prior to final design approval. A working knowledge of the Numonyx™ Flash Memory products specified above is assumed throughout this document. System designers can also review a list of top technical issues on the web at:

http://developer.Numonyx.com/design/flash/support/wireless/index.htm.

This document is based on information available at the time of publication. Any subsequent changes in those specifications may not be reflected in this document. Check with your local Numonyx sales office to have the latest product information before finalizing any design.

2.0 Design Checklist

The top technical design issues have been compiled for Table 1, and can be used as a checklist when designing with these devices. Items can be checked off as they are reviewed. The notes column contains brief design notes and references to other sections of this document with amplifying information. An example memory-interface block diagram is shown in Figure 1, "Block Diagram" on page 7.

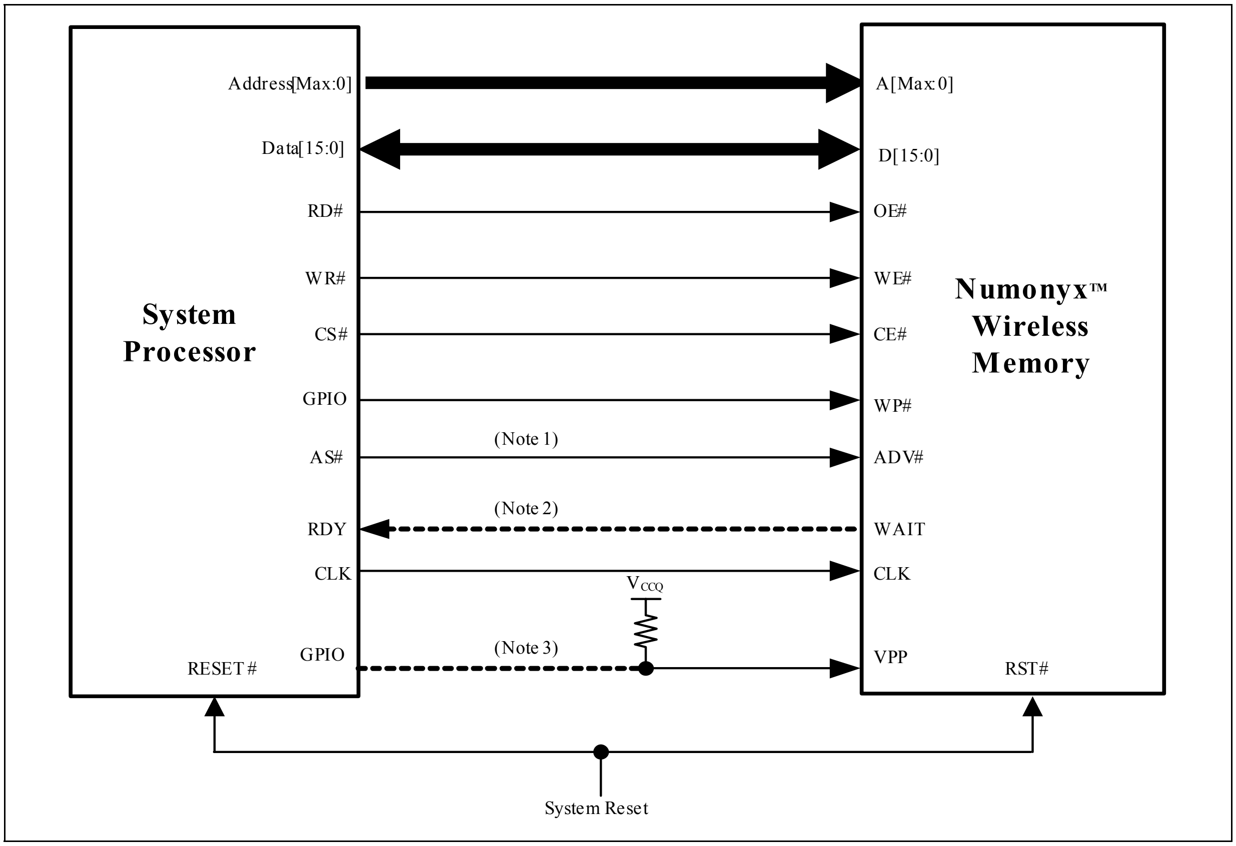
Table 1: Design Checklist (Sheet 1 of 2)

P	Signal	Description	Connection	Notes
	AMin	ADDRESS (Input): Device address inputs for read and write operations. • A_{MIN} = A0	Connect to system address bus.	
	AMax	ADDRESS (Input): Device address inputs for read and write operations. For L18/L30 • 64Mb: A_{MAX} = A21 • 128Mb: A_{MAX} = A22 • 256Mb: A_{MAX} = A23 For W18/W30 • 32Mb: A_{MAX} = A20 • 64Mb: A_{MAX} = A21 • 128Mb: A_{MAX} = A22	Connect to system address bus.	
	D[15:0]	DATA (I/0): Inputs data during writes; outputs data (except Status Register) in reads.	Connect to system data bus.	
	CE#	CHIP ENABLE: (Input): Low-true; CE#-low selects the flash device. CE#-high deselects the device.	Connect to system chip select signal.	CE#-high places data and WAIT outputs at a High-Z level.
	OE#	OUTPUT ENABLE (Input): Low-true; OE#-low enables D[15:0] output buffers during read operations; OE#-high places D[15:0] at High-Z.	Connect to system read-enable signal.	
	WE#	WRITE ENABLE (Input): Low-true; WE#-low controls writes to the device. Address and data are latched on the rising edge of WE#.	Connect to system write-enable signal.	Do not assert WE# and OE# at the same time-unpredictable results can occur.

Table 1: Design Checklist (Sheet 2 of 2)

P	Signal	Description	Connection	Notes
	RST#	RESET (Input): Low-true; RST#-low reset internal automation and places device into power-down mode; RST#-high enables normal operation.	Connect to system reset logic.	Reset flash memory with processor. (See Section 3.5, "Clock (CLK)" on page 8).
	WP#	WRITE PROTECT (Input): Low-true; WP#-low enables the block lock-down mechanism; WP#-high disables the block-lock down mechanism.	Connect to system GPIO.	WP#-high overrides the lock-down function enabling blocks to be erased or programmed through software. WP# can be tied low if the override feature is not preferred. (Section 3.3, "Write Protection (WP#)" on page 8).
	ADV#	ADDRESS VALID (Input): Low-true; during synchronous-burst read operations, addresses are latched on the rising edge of ADV# or on the next valid clock edge ADV#-low, whichever occurs first.	Optional - Connect to system address strobe signal or CE#.	Tie to GND if not used. (See Section 3.4, "Address Valid (ADV#)" on page 8).
	VPP	PROGRAM ENABLE (Power/Input): VPP > VPPLK enables the device to program, erase, and configure block lock bits.	Connect to system program enable logic.	Can be switch-controlled. (See Section 3.7, "Program/Erase Protection" on page 9).
	CLK	CLOCK (Input): Synchronizes the device to the system's bus frequency in synchronous-burst read mode, and increments the internal address generator. Address is latched on a valid CLK edge when ADV# is low or on the rising edge of ADV#, whichever occurs first.	Connect to system clock.	Do not float clock signal. CLK should be tied to a valid VIH if not used. (See Section 3.5, "Clock (CLK)" on page 8).
	WAIT	WAIT (Output): Indicates invalid data in synchronous-read (burst) modes.	Optional – Connect to system Wait state generator or to system data ready signal.	Can be left floating if not used. (See Section 3.6, "WAIT Signal" on page 9).
	VCC	Core (logic) Supply: Normal operations inhibited when VCC < VLKO.	Connect to flash VCC power supply source.	(See Section 3.8, "Power Supply Decoupling" on page 9).
	VCCQ	Output Buffer (I/0) Supply: Provides voltage source for device's output buffers.	Connect to flash VCCQ power supply source.	(See Section 3.8, "Power Supply Decoupling" on page 9).
	VSS	GROUND: Device ground for core power supply.	Connect to system logic (digital) ground.	Do not float any grounds.
	VSSQ	I/O GROUND: Device I/0 ground for I/0 power supply.	Connect to system logic (digital) ground.	Do not float any grounds.
	DU	DO NOT USE.	Do not connect to system.	
	NC	NO CONNECT: No internal connections	Can be driven or floated.	
	RFU	RESERVED for FUTURE USE: Reserved by Numonyx for future device functionality and enhancement.	Do not connect to system.	

Figure 1: Block Diagram



Notes:
1. For connection options, see ADV# in Table 1, "Design Checklist" on page 5.
2. For connection options, see WAIT in Table 1, "Design Checklist" on page 5.
3. For connection options, see VPP in Table 1, "Design Checklist" on page 5.

3.0 Design Considerations

The following sections describe hardware design considerations when designing a system using the Numonyx™ StrataFlash® Wireless Memory (L18/L30) and the Numonyx™ Wireless Flash Memory (W18/W30) devices.

3.1 Upper Address Bits (A[23:20])

Designs using low-density flash memory can be pre-enabled for higher flash memory to support additional premium-product features, or simply to allow for future design growth, such as for increased code size. In either case, the upper address lines used on higher-density flash devices must be considered.

For example, designs using Numonyx™ Wireless Flash Memory (W18, 32-Mbit) can be pre-enabled to support higher-density devices. The most significant address bit (MSB) of the 32-Mbit device is A20, while the MSB of the 64-Mbit and 128-Mbit devices are A21 and A22, respectively. These upper address bits are not connected internally (NC) on the lower density device; therefore, the processor's address bus connections for the upper address bits used on the higher-density devices can be included on lower-density designs. In this way, higher density flash memory that you simply drop-in is compatible with low-density designs.

If a design is using higher-density devices in lieu of lower-density devices, you must ensure the unused MSB address bits are properly terminated. Connections to tie these unused flash memory inputs high or low will depend on the designers preference for which portion of the flash device is to be used in the design, as well as how much flexibility to include for future product designs.

3.2 Reset (RST#)

As with any automated device, it is important to assert RST# during system reset to ensure the flash memory device exits from reset along with the processor. If a CPU reset occurred without resetting the flash memory, proper system initialization may not occur because the flash memory may be providing status information instead of array data (e.g. processor instructions).

The flash memory device is disabled and resets whenever RST# is asserted. The RST# input should be tied to the same reset logic used to reset the system processor. The flash memory device defaults to asynchronous read-array mode after a reset. Also, the internal logic is designed to protect against accidental block erasure, programming, or lock-bit configuration during power transitions.

3.3 Write Protection (WP#)

The flash memory device offers two levels of data protection via software and hardware.

Initially all blocks power-up in a locked state. When WP# is asserted, the lock-down mechanism is enabled and blocks marked lock-down cannot be unlocked through software. When WP# is deasserted, the lock-down mechanism is disabled and blocks previously locked-down are locked through software.

3.4 Address Valid (ADV#)

The address valid (ADV#) is used to latch the initial address during synchronous read operations. ADV#-low opens the device's internal address latches, and informs the device that a valid address is present on the address inputs. When the device is enabled (CE#-low) with ADV#-high, the device does not recognize any address inputs.

ADV# can be tied to CE# if a system processor does not have an address strobe to indicate when the address is valid. In this case, the address will be latched on the next edge of CLK after CE# (ADV#) goes low.

When using the flash in asynchronous mode only, ADV# should be tied to GND.

3.5 Clock (CLK)

The clock input (CLK) is required for synchronous-burst read operations. After ADV# goes low, the initial address is latched on the valid edge of CLK or the rising edge of ADV#, whichever occurs first. CLK is not used during asynchronous reads, or write operations. CLK should be tied to VIH if synchronous burst operation is not used.

3.6 WAIT Signal

The WAIT output signal is provided to ease CPU-to-flash memory communication and synchronization during burst-mode reads. WAIT can be used to provide an input to a CPU's wait-state generator to indicate when a data-sampling delay is necessary, such as during the initial access latency period of the flash memory

The WAIT output signal is programmable through the Read Configuration Register (RCR) bits [CR.10] for WAIT polarity and [CR.8] for WAIT delay.

3.6.1 W18/W30 WAIT

During synchronous array read operations, WAIT is driven with respect to CE#. WAIT indicates invalid data when asserted, and valid data when de-asserted with respect to a valid clock edge.

WAIT is asserted during synchronous non-array reads, asynchronous reads, and all writes. WAIT can be left floating if not used in synchronous mode.

3.6.2 L18/L30 WAIT

During synchronous array and non-array read operations, WAIT is driven with respect to OE# with CE# asserted. WAIT indicates invalid data when asserted, and valid data when de-asserted with respect to a valid clock edge.

WAIT is deasserted during asynchronous reads and all writes. WAIT can be left floating if not used in synchronous mode.

3.7 Program/Erase Protection

System designer should guard against spurious writes whenever VCC is above the VCC lockout voltage, VLKO, and when VPP is active. By keeping VPP below VPPLK when not actively programming or erasing, inadvertent data alteration can be prevented.

VPP can be hard-wired to VPPL or VPP1, or switched between VPPL or VPP1 and GND for optimized data protection. When VPP is less than VPPLK, flash memory contents cannot be altered.

If system designers elect to hard-wire VPP to VPPL or VPP1, the device's block-lock capability and two-cycle command sequence provides a software mechanism that can provide protection from inadvertent code/data alteration. It is important to note that under these conditions, memory contents can still be altered, and is dependent on the stability of the system design.

3.8 Power Supply Decoupling

Flash memory power supplies require careful decoupling. System designers are most interested in three types of power-supply current levels: 1) active current, 2) standby current, and 3) transient peak current cause by rising/falling edges of signals such as CEx and OE#. The latter is the most difficult to control, and the subject of this section.

The magnitude of transient currents is dependent on the flash device's capacitive and inductive loading. Two-line control and proper capacitor selection will help to suppress transient voltage (and current) peaks. The flash device has two VCC pins that supply core logic current and program/erase current to the device. It is recommended that a 0.1uF ceramic capacitor be connected from each VCC pin (and VCCQ) to ground. High-frequency, low-inductance capacitors should be used, and located as close as possible to the device pins. Additionally, 4.7uF electrolytic capacitors should be dispersed about the PCB to overcome voltage slumps caused by circuit board inductance.

3.9 Input Signal Transitions

The use of fast, high-drive transceivers and buffers can cause input signals to exceed device specifications. Transceiver/buffer vendors now offer devices with internal output-damping resistors or reduced-drive outputs that diminish the nominal output-drive currents while still meeting signal-drive requirements for most applications. The damping resistors help to reduce signal overshoot and undershoot by limiting the current into the input of the flash memory.

3.10 Capacitive Loading

Consideration should be given to system bus loading imposed on the device I/O when designing a system. Additional devices connected to the system bus with the flash memory device will increase the capacitive load seen by the flash memory. Increases in capacitive load have the effect of slowing down the rise and fall of signals driven by the flash memory.

The flash memory device is tested to a CLOAD of 30pF. Generally, for every 10pF of additional capacitive load in excess of that specified, adds approximately 1 ns of delay to the access speed specifications. Designers must take this into account when planning a system design.

Appendix A Additional Information

Order Number	Document/Tool
251902-03	Numonyx™ StrataFlash® Wireless Memory (L18); 28F640L18, 28F128L18, 28F256L18 Datasheet
251903-03	Numonyx™ StrataFlash® Wireless Memory (L30); 28F640L30, 28F128L30, 28F256L30 Datasheet
290701-08	Numonyx™ Wireless Flash Memory (W18) - 28F320W18, 28F640W18, 28F128W18 Datasheet
290702-07	Numonyx™ Wireless Flash Memory with 3 Volt I/O (W30); 28F640W30, 28F320W30, 28F128W30 Datasheet
297859-02	AP-677 Numonyx™ StrataFlash® Memory Technology
292222-02	AP-664 Designing Numonyx™ StrataFlash® Memory into Numonyx Architecture
251908-02	AP-753 Migration Guide for Numonyx™ Wireless Flash Memory (W18) to Numonyx™ StrataFlash® Wireless Memory (L18)
251909-02	AP-754 Migration Guide for Numonyx™ Synchronous StrataFlash® Memory (K3) to Numonyx™ StrataFlash® Wireless Memory (L18)
252861-01	AP-773 Numonyx™ StrataFlash® Wireless Memory (L18) to Intel* PXA800F Cellular Processor Design Guide
252267-01	AP-776 Numonyx™ StrataFlash® Wireless Memory (L30) to Intel* PXA250 Applications Processor Design Guide
250260-01	AP-751 System Design Considerations When Designing with Numonyx™ Flash

Note: Contact your local Numonyx distribution sales office or visit Numonyx's World Wide Web home page at http://www.numonyx.com for technical documentation, tools, and for the most current information on Numonyx flash products.