



Conversion Guide : Numonyx[®] Embedded Flash Memory (32, 64 and 128 Mbit) J3 v. D to J3 65 nm

Application Note - 308038

July 2010

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Revision History

Date of Revision	Revision	Description
June 2009	01	Initial Release.
May 2010	02	<p>Added Blank Check information for J3 65nm SBC.</p> <p>Added Blank Check specification tBC/MB, update Clear Block Lock-Bits Max Time and Program time for J3 65nm SBC.</p> <p>Added a note to clarify the SR output after E8 command in Table 1, "J3 v. D vs. J3 65nm SBC Comparison" on page 7.</p> <p>Added Page Mode and ECR.13 comparison.</p> <p>Added device ID information for 32- and 64-Mbit devices in Table 6, "Comparison: Device Identifiers" on page 12.</p>
July 2010	03	Emphasized the valid and legal command usage.

1.0 Introduction

This document is intended to assist customer conversion from the Numonyx® Embedded Memory (J3 v. D) to Numonyx® Embedded Memory (J3 65nm) Single Bit per Cell (SBC) device, including explanation of key hardware and software differences.

Unless otherwise indicated throughout the rest of this document, the Numonyx® Embedded Flash Memory (J3 v. D) device is referred to as J3 v. D and the Numonyx® Embedded Memory (J3 65nm) Single Bit per Cell device is referred to as J3 65nm SBC.

This document was written based on information available at the time. Changes in specifications to the devices may not be reflected in this document. Refer to the appropriate datasheet or sales personnel for the most current information before finalizing any design.

2.0 Device Overview

The following sections provide a brief overview of J3 v. D and J3 65nm SBC devices.

2.1 J3 65nm SBC

The J3 65nm SBC features 32-, 64- and 128-Mbit densities in 64-ball Numonyx® Easy BGA and 56-lead TSOP package. It's advanced features include larger programming buffer, higher security through the new password access feature, individual and instantaneous block locking and block erase/program lockout during power transitions.

2.2 J3 v. D

The J3 v. D device is offered in 32-, 64- and 128-Mbit densities. Their security features include OTP Protection, Individual and Instantaneous Block Locking. This family brings reliable, low-voltage capability (3 V read, program, and erase) with high speed, low-power operation. These devices are available in 64-Ball Easy BGA package and 56-lead TSOP package.

2.3 J3 v. D vs. J3 65nm SBC Feature Comparison

Table 1: J3 v. D vs. J3 65nm SBC Comparison

Feature	J3 v. D	J3 65nm SBC
Density	32, 64, 128 Mbit	32, 64, 128 Mbit
V _{CC}	2.7V-3.6V	2.7V-3.6V
TSOP	Yes	Yes
Easy BGA	Yes	Yes
Initial Access Time	75 ns (32, 64, 128 Mbit)	75 ns (32, 64, 128 Mbit)
Async Page	25 ns	25 ns
Protection Register	128 bits	128 bits
Bus width	x8/x16	x8/x16
Multiple Chip Enables	Yes (CE[2:0])	Yes (CE[2:0])
Architecture	Single bit per cell	Single bit per cell
Security and protection	128-bit Protection Register Normal Block Locking — Non-Volatile Modify Protection (temporary) Configurable Block Locking — Non-Volatile Modify Protection (semi-permanent or permanent)	128-bit Protection Register Normal Block Locking — Non-Volatile Modify Protection (temporary) Configurable Block Locking — Non-Volatile Modify Protection (semi-permanent or permanent) Password Access — Non-Volatile Read and Modify Protection
Temperature	-40 °C to +85 °C	-40 °C to +85 °C
Program Suspend	Yes	Yes
Erase Suspend	Yes	Yes
Process	130 nm	65 nm
Buffer Program Size ²	32-Byte (x8 mode) 16-Word (x16 mode)	256-Byte (x8 mode) ¹ 256-Word (x16 mode) ¹
Block Size	128 KB	128 KB
Word Program	40 μs	40 μs
Erase	1 s	1 s
Page Mode Reads Page Size	4 Words / 8 Words	8 Words / 8 Words
Power-up Timing	60 μs	60 μs
CFI Compatible	Yes	Yes
Blank Check	No	Yes

Notes:

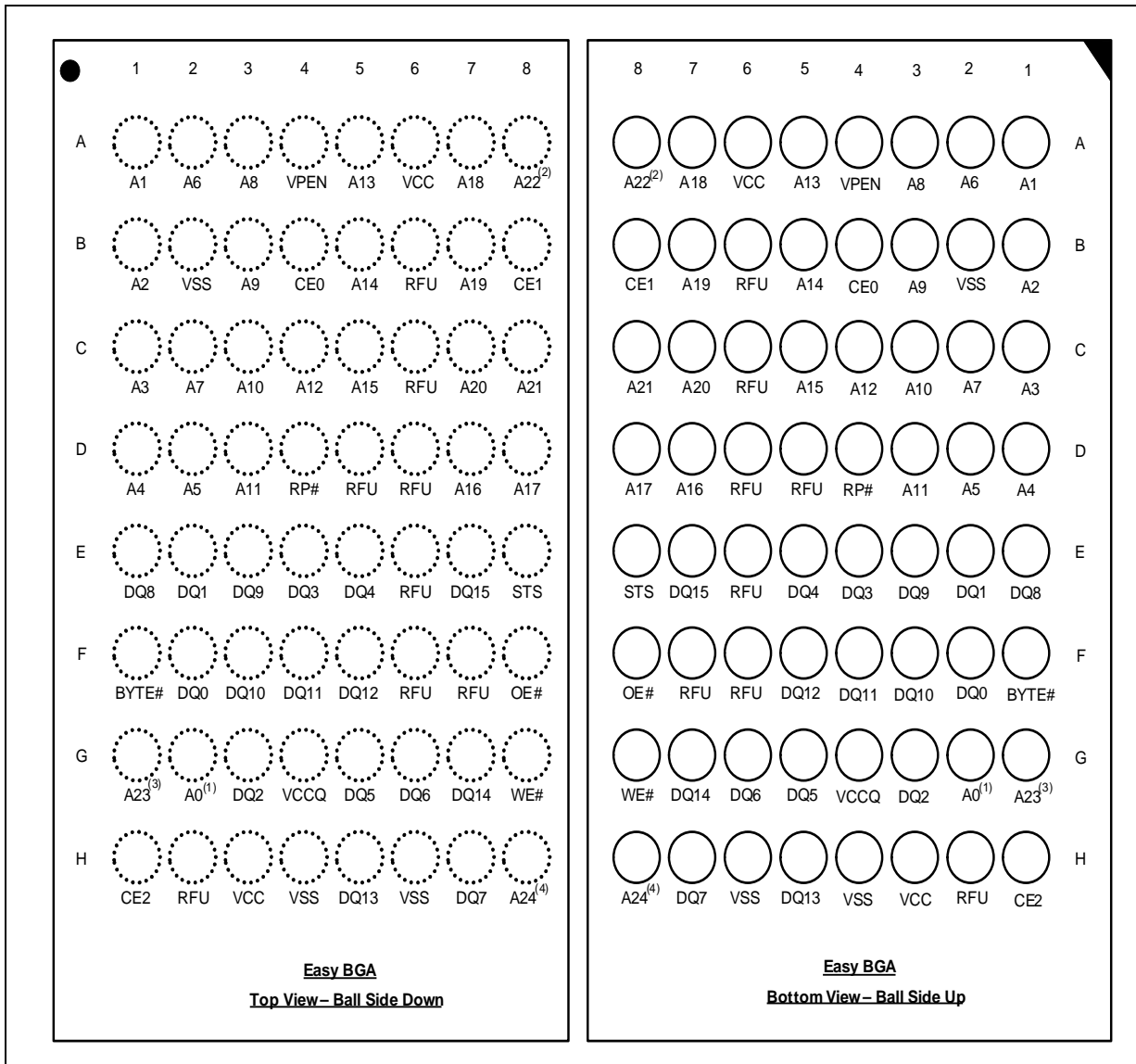
1. For the backward compatibility, value 05 (32-Byte/16-Word) is put on CFI Device Geometry Definition for maximum number of bytes in write buffer (offset: 0x2Ah).
2. The device defaults to output SR data after the Buffered Programming Setup command (E8h) is issued. CE# and OE# must be toggled to update Status Register. Don't issue the Read SR command (70h) because it would be interpreted by the internal state machine as Buffer Word Count.

3.0 Device Ballout and Signal Descriptions

3.1 64-Ball Numonyx® Easy BGA Ballout

The 64-Ball Numonyx® Easy BGA ballout is the same for both J3 v. D and J3 65nm SBC products.

Figure 1: Numonyx® Easy BGA Ballout



Notes:

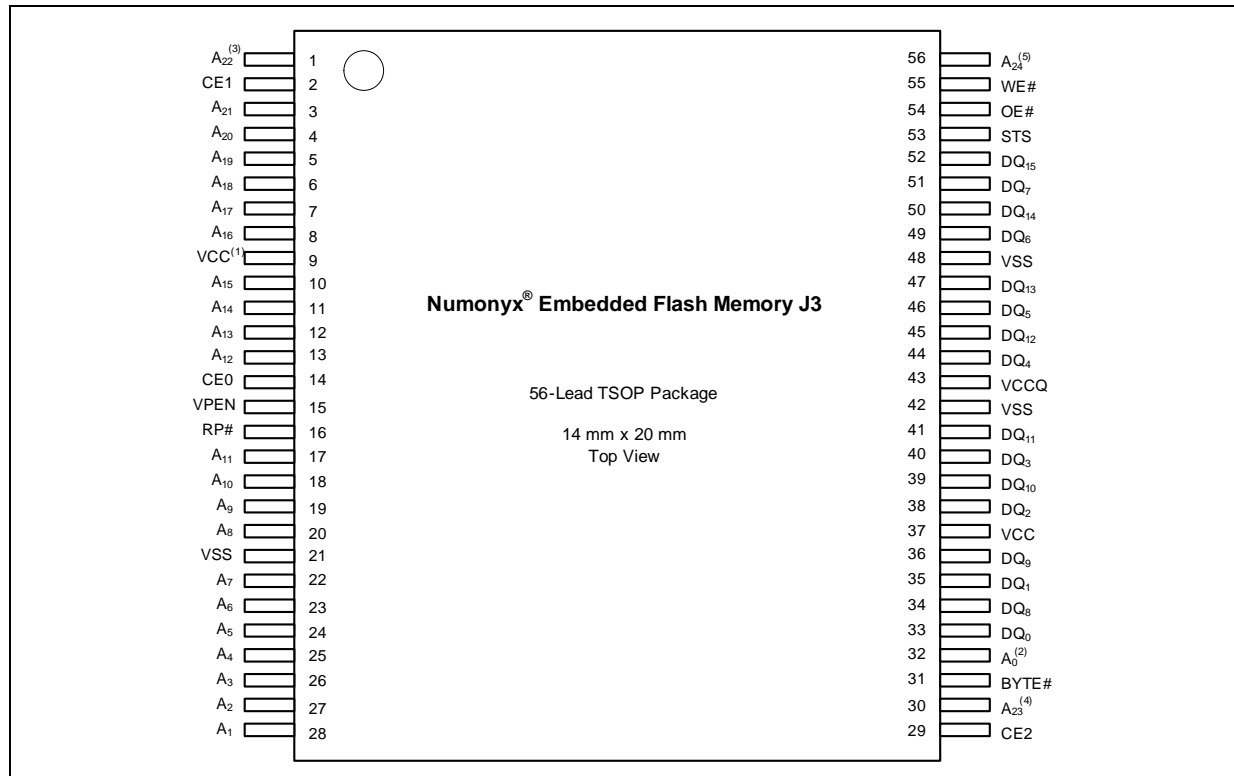
1. A0 is the least significant address bit.
2. Address A22 is only valid for 64-Mbit density and above, otherwise it is a no connect (NC).
3. Address A23 is only valid for 128-Mbit density and above, otherwise it is a no connect (NC).
4. Address A24 is a no connect (NC) on 128-, 64-, 32-Mbit, reserved for 256-Mbit.

3.2 56-Lead TSOP Pinout

The TSOP pinout is compatible for both J3 v. D and J3 65nm SBC products.

Pin 9 on J3 v. D is connected to Vcc. For J3 65nm SBC this pin has no internal connection; it may be driven or left floating.

Figure 2: 56-Lead TSOP 14 mm x 20 mm:



Notes:

1. No internal connection for pin 9 of J3 65nm SBC; it may be driven or floated. For legacy designs, pin 9 can be tied to V_{CC}.
2. A₀ is the least significant address bit.
3. Address A₂₂ is only valid for 64-Mbit density and above, otherwise it is a no connect (NC).
4. Address A₂₃ is only valid on 128-Mbit density and above, otherwise it is a no connect (NC).
5. Address A₂₄ is a no connect (NC) on 128-, 64-, 32-Mbit, reserved for 256-Mbit.

3.3 Signal Descriptions

The signal description is the same for both J3 v. D and J3 65nm SBC products.

4.0 Hardware Design Considerations

The following section discusses hardware design considerations when converting from J3 v. D to J3 65nm SBC.

4.1 AC Read/Write Specifications

The AC read/write specifications are the same for both J3 v. D and J3 65nm SBC device. See the following tables for key AC Read and Write Specifications.

Table 2: Comparison: Key AC Read Specifications

Symbol	Specification	Density	J3 v. D	J3-65 SBC
t_{AVAV}	Read Cycle time	All	75 ns	75 ns
t_{AVQV}	Address to output delay		75 ns	75 ns
t_{ELQV}	CE# low to Output Valid		75 ns	75 ns
t_{GLOV}	OE# to Non-Array Output Delay		25 ns (max)	25 ns (max)
t_{PHQV}	RP# High to Output Delay	32 Mbit	150 ns	150 ns
		64 Mbit	180 ns	180 ns
		128 Mbit	210 ns	210 ns
t_{EHOZ}	CEX High to Output in High Z	All	25 ns	25 ns

Table 3: Comparison: Key AC Write Specifications

Symbol	Specification	Density	J3 v. D	J3-65
t_{PHWL} (t_{PHEL})	RP# high recovery to WE# (CEX) going low.	32 Mbit	150 ns	150 ns
		64 Mbit	180 ns	180 ns
		128 Mbit	210 ns	210 ns
t_{WP}	Write pulse width	All	60 ns	60 ns
t_{AVWH}	Address Setup to WE# (CEX) Going High		55 ns	55 ns
t_{WPH} t_{WHWL}	Write Pulse Width High		30 ns	30 ns
t_{WHGL}	Write Recovery before Read		35 ns	35 ns
t_{WHRL} t_{EHRL}	WE# (CEX) High to STS Going Low		500 ns (max)	500 ns (max)

4.2 DC Specifications

The DC specs are the same for both J3 v. D and J3 65nm SBC products. See the following table for details.

Table 4: DC Current and Voltage Specifications

Symbol	Specification	J3 v. D	J3 65nm SBC
I_{CCS}	V _{CC} Standby current	50 uA (typ) / 120 uA (max)	50 uA (typ) / 120 uA (max)
I_{CCR}	Page Mode Read Current (8-Word Page 33Mhz)	54 mA (max)	54 mA (max)
I_{CCW}/I_{CCE} (typ and max)	V _{CC} Program or Set Lock-Bit Current	40 mA (typ) / 70 mA (max)	40 mA (typ) / 70 mA (max)
V_{IL}	Input Low Voltage	-0.5 V (min) / 0.8 V (max)	-0.5 V (min) / 0.8 V (max)
V_{LKO}	V _{CC} Lockout Voltage	2.0 V	2.0 V

4.3 Capacitance

The below table lists the capacitance difference between J3 v. D and J3 65nm SBC. The slight difference for Input/Output Capacitance won't impact customer's hardware.

Table 5: Difference: Capacitance

Symbol	Parameter	J3 v. D		J3 65nm SBC	
		Typ	Max	Typ	Max
C_{IN}	Input Capacitance	6pF	8pF	6pF	7pF
C_{OUT}	Output Capacitance	8pF	12pF	4pF	5pF

5.0 Software Design Considerations

The following sections discuss software design considerations when converting from the J3 v. D device to the J3 65nm SBC device.

5.1 Device Identifiers

The J3 65nm SBC device contains the same device identifiers as the J3 v. D device.

Table 6: Comparison: Device Identifiers

Code Type	Device Address ⁽¹⁾	Density	J3 v. D	J3-65 SBC
Manufacturer Code	0x00	All	0089h	0089h
Device Code	0x01	32 Mbit	0016h	0016h
		64 Mbit	0017h	0017h
		128 Mbit	0018h	0018h

Note: Numonyx reserves other locations within the Identifier address space for future use.

5.2 Device Commands

The command set for J3 v. D and J3 65nm SBC are compatible. J3 65nm SBC device provides additional commands for the enhanced security features: Password Access Protection. Please contact your Numonyx sales for the details. J3 65nm SBC device also provides the Blank Check command to verify an erased block.

Note: Some customer applications use illegal or invalid commands (like 0x00) accidentally or intentionally with the device. An illegal or invalid command caused the device output to change to Array Read mode on 130nm. On the 65nm device, the output will change to Read Status Register mode.

After an illegal or invalid command, software may attempt to read the device. If the illegal command was intentional, software will expect to read array data on 130nm device, such as 0xFFFF in an unprogrammed location. On the 65nm device, software may not get the expected array data and instead the status register is read.

Please refer to the legal and valid commands/spec defined in the Datasheet, such as for read mode, issue 0xFF to Read Array mode, 0x90 to Read Signature, 0x98 to Read CF1/OTP array mode.

5.3 Page mode and Enhanced Configuration Register

J3 v. D device provides both Four-Word Page Mode and Eight-Word Page Mode. ECR.13 selects between these two Page Modes. J3 65nm SBC device provides Eight-Word Page Mode only because the device stays in Eight-Word sensing no matter what ECR[13] is configured.

Table 7: Difference for page mode and ECR.13

Symbol	Data	J3 v. D	J3 65nm SBC
ECR.13	0	4 word page mode (default)	8 word page mode (default)
	1	8 word page mode	8 word page mode

5.4 Program Performance Improvements in J3 65nm SBC

The programming performance is improved on J3 65nm SBC because of its 256-Word (x16 mode) / 256-Byte(x8 mode) buffer. Software modification is not required if the application uses 16-Word(x16 mode) or 32-Byte(x8 mode) buffer size just like on J3 v. D devices.

Using the full 256-Word(x16 mode) / 256-Byte(x8 mode) buffer size is the best choice of the fastest programming performance. Optimal performance and power consumption are realized by aligning the start address on 256-Word boundaries. Crossing a 256-Word boundary during a buffered programming operation can double the programming time.

Table 8: Difference: Program/Erase/Block Lock Specifications

Symbol	Specification	J3 v. D	J3 65nm SBC
$t_{\text{PROG/B}}$	Aligned 16-word Buffered Program Time	128 μs (typ) 654 μs (max)	128 μs (typ) / 654 μs (max)
	Aligned 256-word Buffered Program Time	NA	720 μs (typ) / 3600 μs (max)
t_{lkC}	Clear Block Lock-Bits Time	0.5 Sec (typ)/ 0.7 Sec (max)	0.5 Sec (typ)/ 1 Sec (max)
$t_{\text{BC/MB}}$	Blank Check Time	NA	3.2ms (typ)
t_{VCCPH}	Vcc Power Valid to RP# de-assertion (high)	60 μs	60 μs
t_{STS}	STS Pulse Width Low Time (Typ)	500 ns	500 ns
t_{WHQV3} t_{EHQV3}	Word Program (Typ)	40 μs	40 μs
	Word Program (Max)	175 μs	175 μs
t_{WHQV4} t_{EHQV4}	Block Erase Time (Typ)	1 s	1 s
	Block Erase Time (Max)	4 s	4 s
t_{WHRH1} t_{EHRH1}	Program Suspend Latency Time to Read (Typ)	15 μs	15 μs
	Program Suspend Latency Time to Read (Max)	20 μs	20 μs
t_{WHRH} t_{EHRH}	Erase Suspend Latency Time to Read (Typ)	15 μs	15 μs
	Erase Suspend Latency Time to Read (Max)	20 μs	20 μs

5.5 Read and Modify Password Access Protection

Password Access is a security enhancement offered on the J3 65nm SBC device. This feature protects information stored in main-array memory blocks by preventing content alteration or reads, until a valid 64-bit password is received. Password Access may be combined with Flexible Block Locking and/or Configurable Block Locking to create a multi-tiered solution.

Please contact your Numonyx Sales Representative for further details concerning Password Access.

5.6 CFI Differences

During adoption of Numonyx® or third party software, several differences must be taken into account. This section will describe the changes.

5.6.1 System Interface Information

The following device information can optimize system interface software. All changes between J3 v. D and J3 65nm SBC are noted in table below.

Table 9: System Interface Information

Offset	Length	Description	Address	J3 v. D		J3 65nm SBC	
				Hex Code	Value	Hex Code	Value
1Fh	1	"n" such that typical single word program time-out = 2 ⁿ μ-sec	1F	06	64 μs	06	64 μs
20h	1	"n" such that typical max. buffer write time-out = 2 ⁿ μ-sec.	20	07	128 μs	07	128μs ¹
23h	1	"n" such that maximum word program time-out = 2 ⁿ times typical	23	02	256 μs	02	256 μs
24h	1	"n" such that maximum buffer write time-out = 2 ⁿ times typical	24	03	1024 μs	03	1024μs ¹
Notes:							
1. Values comprehended for 32-Byte buffer write.							

5.6.2 Device Geometry

This field provides critical details of flash device geometry.

Table 10: Device Geometry Definition

Offset	Length	Description	Address	J3 v. D		J3 65nm SBC	
				Hex Code	Value	Hex Code	Value
2Ah	2	"n" such that maximum number of bytes in write buffer = 2 ⁿ	2A	05	32 bytes	05	32 bytes ¹
Notes:							
1. For backward compatibility, the J3 65nm SBC device is capable for 256-Byte (x8 mode) / 256-Word (x16 mode).							

5.6.3 Read Information

This field provides critical details of the page mode read capability.

Table 11: Read Information

Offset P = 31	Length	Description	Address	J3 v. D		J3 65nm SBC	
				Hex Code	Value	Hex Code	Value
(P+13) h	1	page mode read capability. "n" such that 2 ⁿ HEX value represents the number of read-page bytes.	44	03	8 bytes	04	16 bytes

6.0 Summary

This application note enables customers to understand the hardware and software differences between the J3 v. D and J3 65nm SBC flash memory devices. Please refer to the relevant datasheet for additional information.

Order/Document Number	Document/Tool
316577	Numonyx® Embedded Flash Memory (J3 v. D) Datasheet.
208032	Numonyx® Embedded Memory (J3 65nm) Single Bit per Cell (SBC) Datasheet.

Note: Contact your local Numonyx or distribution sales office or visit Numonyx's World Wide Web home page at <http://www.Numonyx.com> for technical documentation, tools, and additional information.