



# **Conversion Guide: Numonyx<sup>®</sup> Axcell<sup>™</sup> Flash Memory P30 Stack 256-Mbit/256-Mbit (130nm) to 512-Mbit monolithic (65nm)**

**Application Note - 309044**

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*Apr 2010*

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## Revision History

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Date of Revision	Revision	Description
Aug 2009	01	Initial Release.
Mar 2010	02	Update on TSOP package with VCCQ and Temp. Highlight the difference between the stack and monolithic die. Update the program performance. Update the erase suspend latency. Correct Device ID change comments. Add burst boundary and RCR setting comments. Clarify the buffer program status polling. CFI update aligned with performance update. CFI link area removal.
Apr 2010	03	Tie ADV# to Vss or driven to low for TSOP usage. Full corner applies to TSOP package. Burst Latency Count update. BEFP setup time update.

## 1.0 Introduction

This application note describes the migration from the Numonyx<sup>®</sup> Axcell<sup>™</sup> Flash Memory P30 256-Mbit/256-Mbit 130nm device to the Numonyx<sup>®</sup> Axcell<sup>™</sup> Flash Memory P30 512-Mbit monolithic 65nm device.

*Note:* Unless otherwise indicated, throughout the rest of this document, the Numonyx<sup>®</sup> Axcell<sup>™</sup> Flash Memory P30 256-Mbit/256-Mbit 130nm device is referred to as the P30 Stack 130nm device and the Numonyx<sup>®</sup> Axcell<sup>™</sup> Flash Memory P30 512-Mbit Monolithic 65nm device is referred to as the P30 512-Mbit monolithic 65nm device.

This document was written based on device information available at the time. Any changes in specifications to either device might not be reflected in this document. Refer to the appropriate documents or sales personnel for the current product information before finalizing any design.

## 2.0 Device Overview

The following sections provide a brief overview of the feature differences between the P30 Stack 130nm device and the P30 512-Mbit monolithic 65nm devices.

### 2.1 P30 Stack 130nm Device

The P30 Stack 130nm device employs a Virtual Chip Enable which combines two 256-Mbit die with common chip enable (CE# for Easy BGA and TSOP, or F1-CE# for QUAD+ package). Address A25 (Easy BGA and TSOP package) or Address A24 (QUAD+ package) is then used to select between the die pair with CE# or F1-CE# asserted, depending upon the package option used. When chip enable is asserted and A25 of Easy BGA or TSOP (A24 of QUAD+) is low ( $V_{IL}$ ), the lower 256-Mbit die is selected; when chip enable is asserted and A25 of Easy BGA or TSOP (A24 of QUAD+) is high ( $V_{IH}$ ), the upper 256-Mbit die is selected.

*Note:* A1 is the least significant address bit for TSOP and BGA, A0 for QUAD+ package.

P30 130nm device features include high performance synchronous-burst read, Buffered Enhanced Factory Programming (BEFP) with a 32-word buffer, and an expanded OTP register space.

### 2.2 P30 512-Mbit Monolithic 65nm Device

This P30 512-Mbit monolithic device features high-performance synchronous-burst read mode on Easy BGA package, dramatical improvement in buffer program time with 512-word buffer, flexible security options on single die.

## 2.3 P30 Stack 130nm and Monolithic 65nm Features Comparison

**Table 1: P30 Stack 130nm and Monolithic 65nm Feature Comparison**

Features / Specifications		P30 Stack 130nm	P30 Monolithic 65nm
<b>Die Organization</b>	512 Mbit	Stack (256-Mbit/256-Mbit)	Monolithic (512-Mbit Single Die)
<b>Performance</b>	Synchronous Read <sup>(2)</sup>	52 MHz (Easy BGA) 40 MHz (TSOP)	52 MHz (Easy BGA) NA (TSOP)
	Asynchronous Page Read <sup>(2)</sup>	25 ns	25 ns (Easy BGA) NA (TSOP)
	Initial Access Time (Easy BGA)	88 ns	100 ns
	Initial Access Time (TSOP)	95 ns	110 ns
<b>Block Architecture</b>	Parameter Blocks	Total Eight 32-KByte Blocks (Four on Top and Four on Bottom)	Four 32-KByte with Top or Bottom Configuration; Or Symmetrical Configuration
	Main Blocks	128-kByte	128-kByte
	16-bit data bus	Yes	Yes
<b>Operating Voltage</b>	Logic Core (V <sub>CC</sub> )	1.7 V to 2.0 V	1.7 V to 2.0 V
	I/O (V <sub>CCQ</sub> )	1.7 V to 3.6 V	1.7 V to 3.6 V
<b>Features</b>	OTP Register Space	128-bits + 2 Kbits	128-bits + 2 Kbits
	Flexible Block Locking	Yes	Yes
	Buffered Enhanced Factory Program	32-word buffer	512-word buffer
	Password Access	No	Yes
	Blank Check	No	Yes
<b>Reliability</b>	Operating Temperature	-40 °C to +85 °C	-40 °C to +85 °C
	Cycles	100,000	100,000

**Notes:**

1. This document just covers 512-Mbit die information. For other densities information, please refer to Numonyx local Sales for detail.
2. For synchronous read mode and asynchronous page read mode option with TSOP package, please ask Numonyx local Sales for detail.

### 3.0 Memory Map Comparison

Flash erasing is performed on a block basis. An entire block is erased each time. P30 256-Mbit/256-Mbit stack 130nm device consists of 518 separate blocks (4 Parameter blocks + 510 main blocks + 4 Parameter blocks). Please refer to Figure 1, "Memory Map of P30 Stack 130nm (256-Mbit/256-Mbit)" for detail.

P30 monolithic 512-Mbit 65nm device provides more options. Please refer to Figure 2, "Memory Map of P30 Monolithic 65nm (512-Mbit)" for detail. During the migration from P30 256-Mbit/256-Mbit stack 130nm to monolithic 512-Mbit 65nm, customers can choose Top, bottom or symmetrically-blocked configuration according to the usage model.

**Figure 1: Memory Map of P30 Stack 130nm (256-Mbit/256-Mbit)**

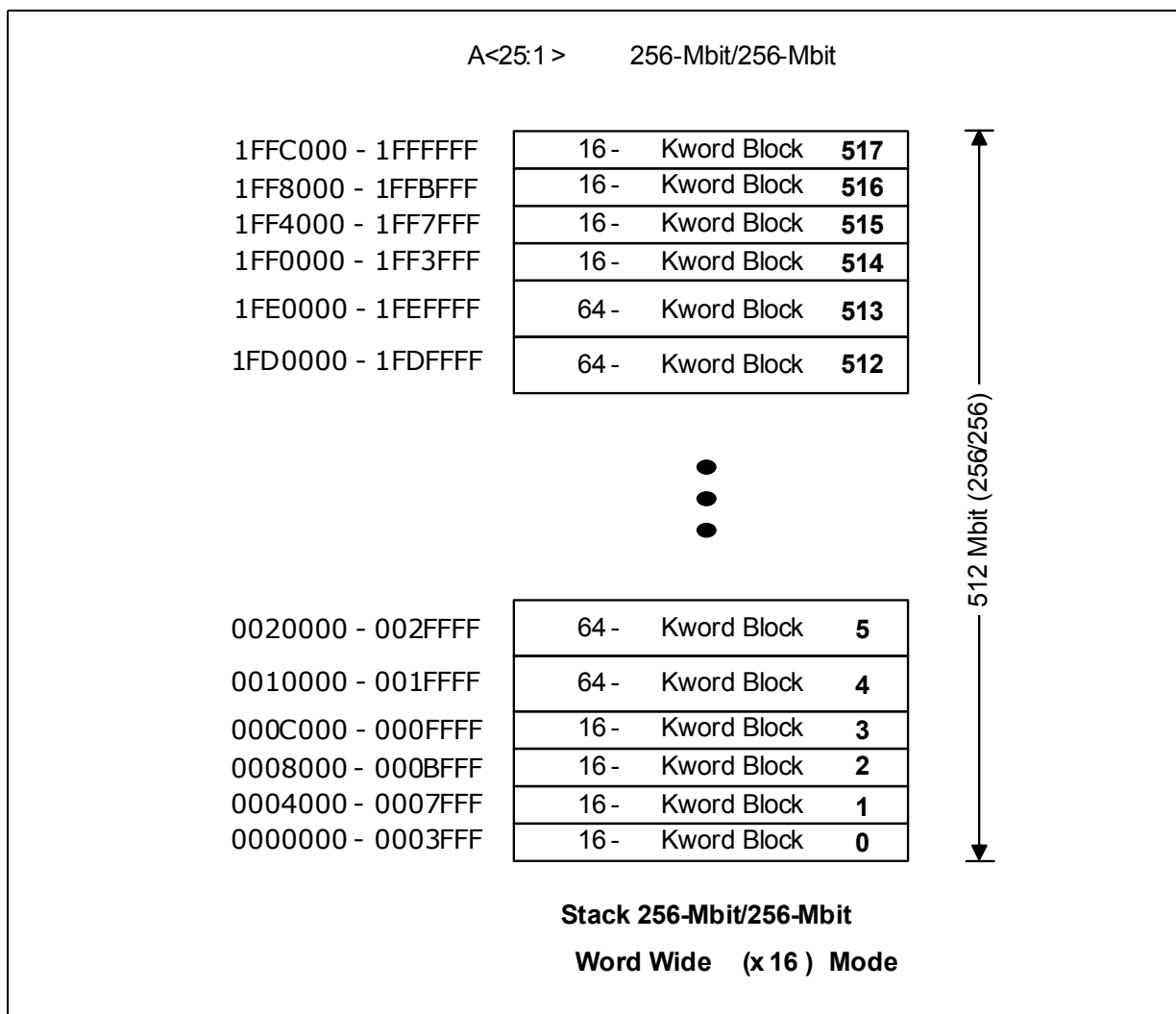
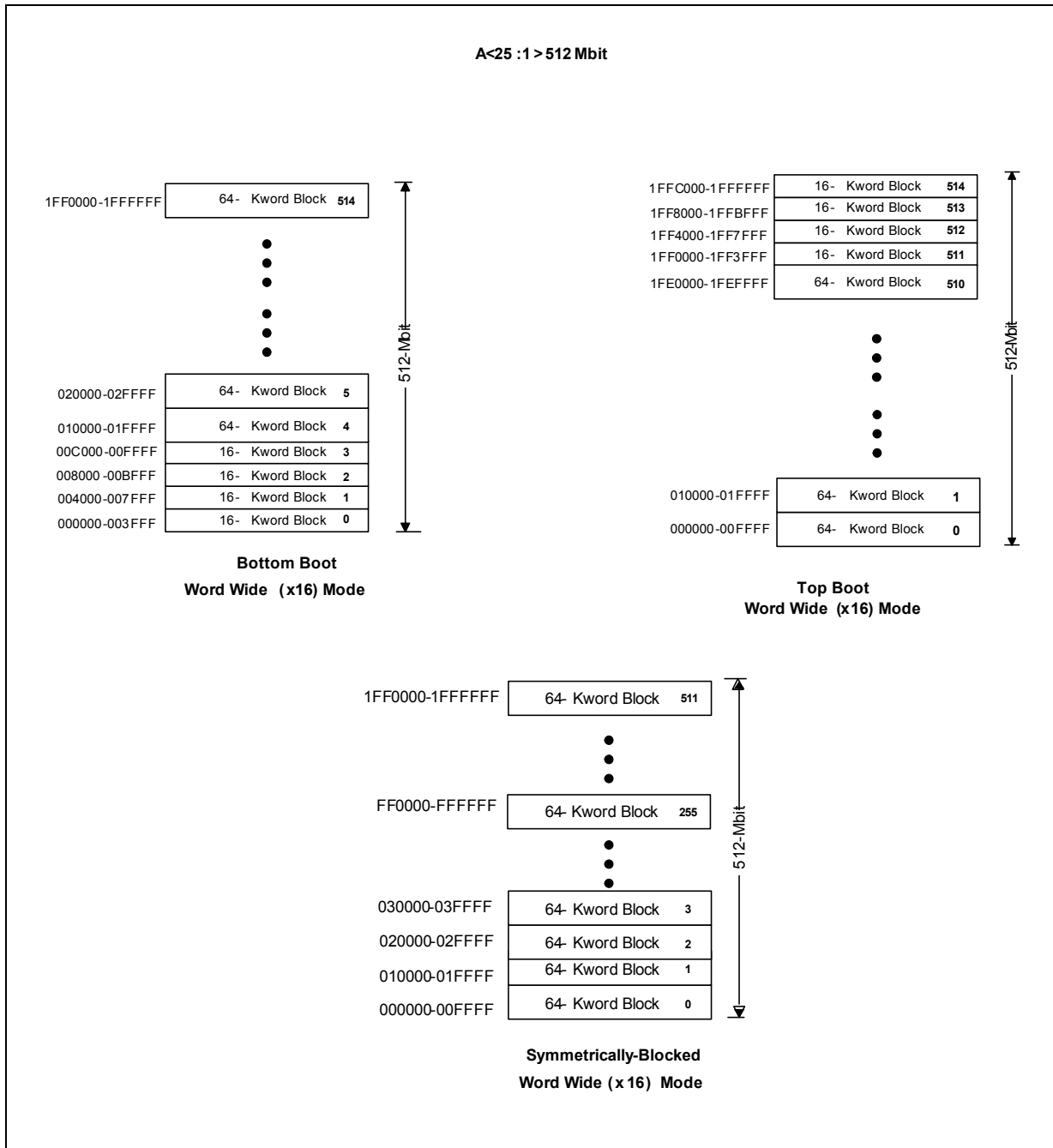


Figure 2: Memory Map of P30 Monolithic 65nm (512-Mbit)



## 4.0 Device Packaging and Ballout

The following section provides a brief overview of the package and ballout differences between the P30 Stack 130nm and P30 monolithic 65nm devices.

**Table 2: Package Comparison**

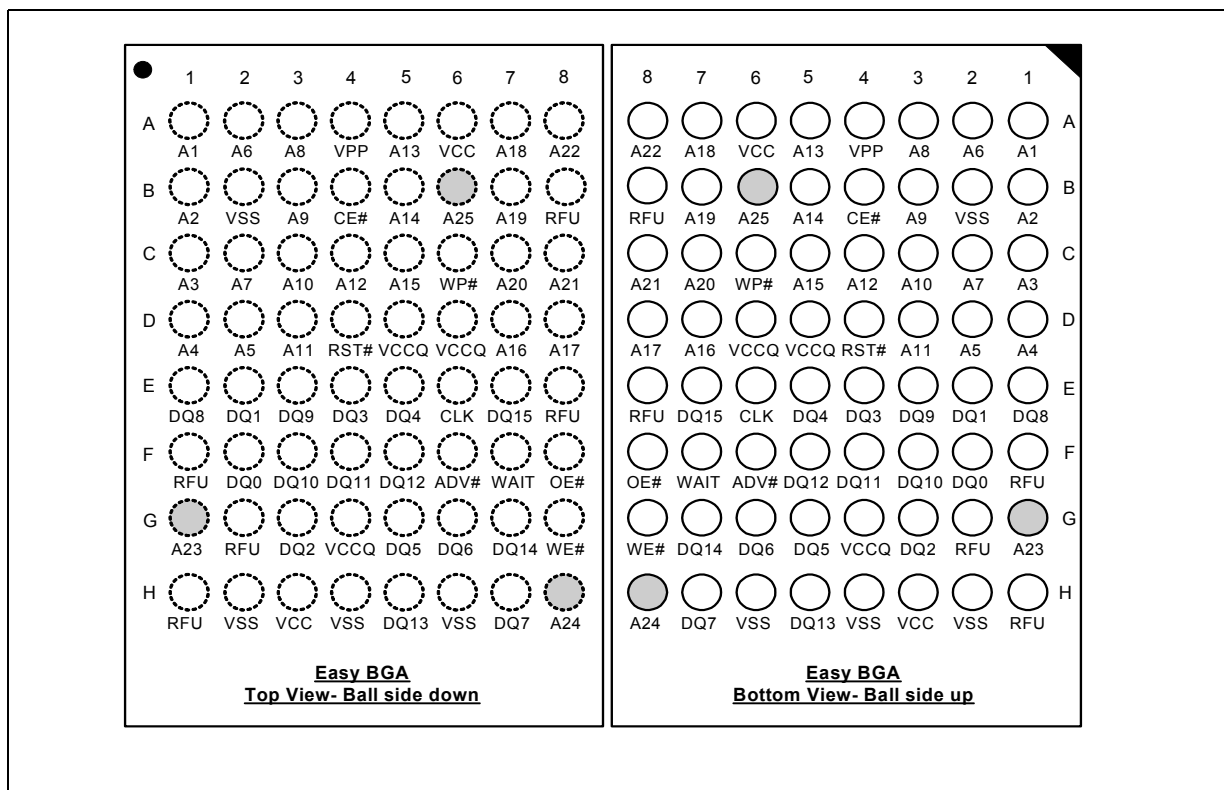
Features / Specifications		P30 Stack 130nm	P30 Monolithic 65nm
512-Mbit Density	Easy BGA	Yes (10x13x1.3 mm)	Yes (8x10x1.2 mm)
	TSOP	Yes	Yes
	QUAD+ (SCSP)	Yes	No

### 4.1 64-Ball Easy BGA Mechanical Specifications and Ballout

The Easy BGA ballout and ball size are same for both P30 Stack 130nm and P30 monolithic 65nm products. Ball pitch of the Easy BGA ballout is 1.0 mm. The package has an 8 x 8 active-ball matrix. However please be aware that P30 stack 130nm body size (10x13x1.3 mm) is different from P30 monolithic 65nm product (8x10x1.2 mm). Refer to the product datasheet for detailed specifications:

- Numonyx® Axcell™ Flash Memory (P30-130nm) Datasheet (306666)
- Numonyx® Axcell™ Flash Memory (P30-65nm Monolithic) Datasheet (208042)

**Figure 3: 64-Ball Easy BGA Ballout**



**Notes:**

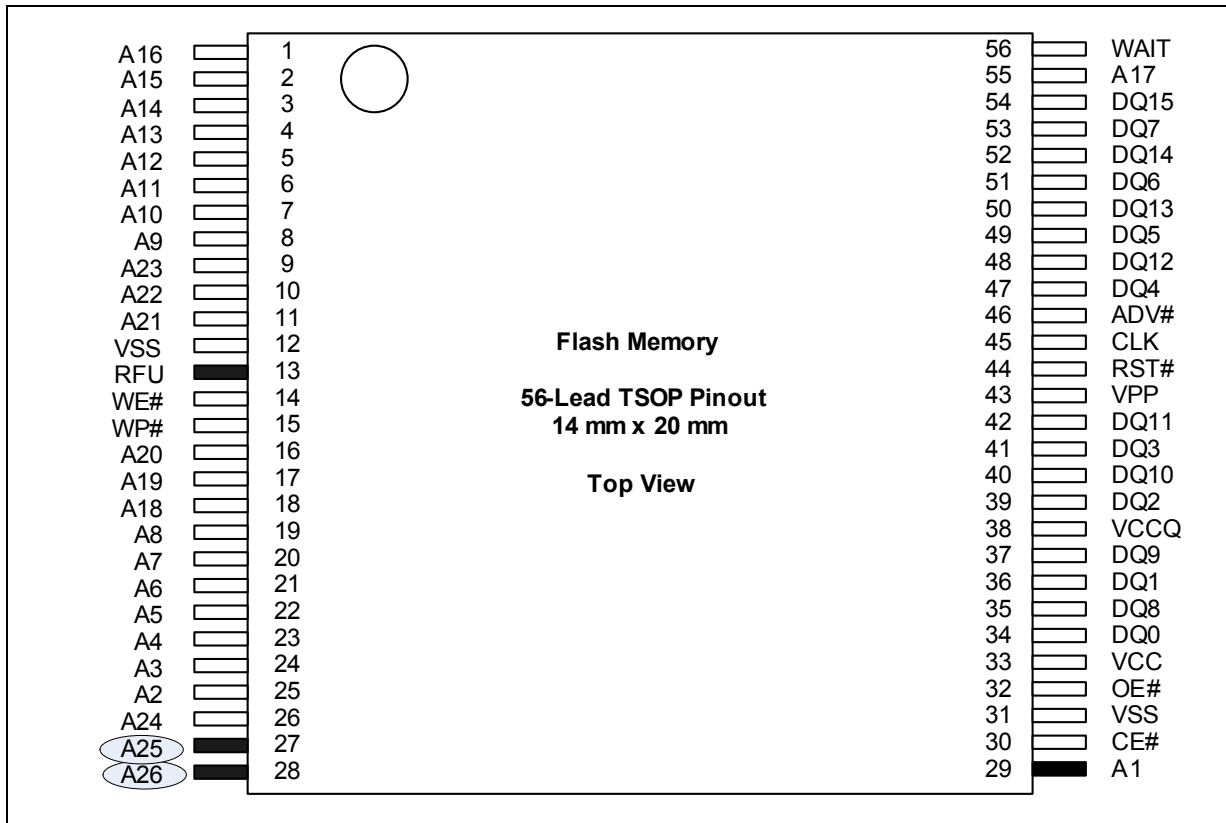
1. A1 is the least significant address bit.
2. A25 is valid for 512-Mbit densities; otherwise, it is a no connect (NC).
3. One dimple on package denotes A1 Pin which will always be in the upper left corner of the package, in reference to the product mark.

## 4.2 TSOP Pinout

The TSOP Pinout is available and compatible for both P30 stack 130nm and P30 monolithic 65nm products. Pin 13 on P30 130nm is connected to Vcc. For P30 65nm this pin has no internal connection; it may be driven or left floated. ADV# must be tied to Vss or driven to low throughout the asynchronous read mode on P30 65nm device.

**Note:** For synchronous read mode and asynchronous page read mode option with TSOP package, please ask Numonyx local Sales for detail.

**Figure 4: 56-Lead TSOP Pinout**



**Note:**

1. A1 is the least significant address bit.
2. ADV# must be tied to Vss or driven to low during the asynchronous read mode.
3. A25 is valid for 512-Mbit densities and above; otherwise, it is a no connect (NC).
4. A26 is valid for 1-Gbit densities; otherwise, it is a no connect (NC).
5. No Internal Connection on Pin 13; it may be driven or floated. For legacy designs, this pin can be tied to Vcc.
6. One dimple on package denotes Pin 1 which will always be in the upper left corner of the package, in reference to the product mark.

## 5.0 Hardware Design Considerations

The P30 stack 130nm and P30 monolithic 65nm flash memory devices provide reliable, two-bit-per-cell storage technology for embedded applications. They satisfy the need for more density in less space, with a high-speed interface. The following sections discuss hardware design considerations when converting from the P30 stack 130nm device to the P30 monolithic 65nm device.

### 5.1 AC Read Specifications

Refer to the product datasheet for detailed list of all read timing specifications:

- Numonyx® Axcell™ Flash Memory (P30-130nm) Datasheet (306666)
- Numonyx® Axcell™ Flash Memory (P30-65nm Monolithic) Datasheet (208042)
- Numonyx® Axcell™ Flash Memory (P30/P33-65nm) Spec Update (509045)

**Table 3: Key AC Read Specification Comparison**

Features / Specifications		P30 130nm	P30 65nm
Performance	Clock Frequency (Max)	52 MHz (Easy BGA) 40 MHz (TSOP)	52 MHz (Easy BGA) NA (TSOP)
	Asynchronous Access ( $t_{AVQV}$ $t_{VLQV}$ $t_{ELQV}$ )	Easy BGA: 85 ns	Easy BGA: 100 ns
		TSOP: 95 ns	TSOP: 110 ns
	Asynch Page Access time ( $t_{APA}$ ) <sup>(2)</sup>	25 ns	25 ns
	Clock-to-Data Burst Access ( $t_{CHQV}$ ) <sup>(2)</sup>	17 ns (52 MHz)	17 ns (52 MHz)
	Burst Data Hold Time ( $t_{CHQX}$ ) <sup>(2)</sup>	3 ns (52 MHz)	3ns (52 MHz)
	Address and ADV# Setup Time ( $t_{AVCH}$ , $t_{VLCH}$ ) <sup>(2)</sup>	9 ns	9 ns
	CE# Setup Time ( $t_{ELCH}$ )	9 ns	9 ns
	Rise/Fall Time ( $t_{FCLK/LCLK}$ )	3.0 ns	3.0 ns
	Clock High/Low Time ( $t_{CH/CL}$ ) <sup>(2)</sup>	5 ns	5ns
	Vcc power valid to RST# de-assertion (high)	60 us	300 us <sup>(1)</sup>
	Async Page Size <sup>(2)</sup>	4 words	16 words
	Synchronous Burst Length (word) <sup>(2)</sup>	4-, 8-, 16-, and Cont.	4-, 8-, 16- and Cont.
	Burst Suspend Mode <sup>(2)</sup>	Yes	Yes
<b>Notes:</b>			
1. Customers need to evaluate your own system power-up timing setting on a real case to meet the specification.			
2. These specs are valid only for Easy BGA package on P30 65nm device.			

### 5.2 AC Write/Erase Specifications

**Note:** Refer to the product datasheet for detailed list of all write and erase timing specifications.

- Numonyx® Axcell™ Flash Memory (P30-130nm) Datasheet (306666)
- Numonyx® Axcell™ Flash Memory (P30-65nm) Datasheet (208042)

**Table 4: Key AC Write-Erase Specification Comparison**

Features / Specifications		P30 130nm	P30 65nm
<b>Program Performance<sup>(1)(2)</sup></b>	Program Buffer Size	64 Bytes	1024 Bytes
	Single Word Program Time (typ/max)	90/200 $\mu$ s	270/456 $\mu$ s
	Aligned 32-word Buffered Program Time (typ/max)	440 $\mu$ s/880 $\mu$ s ( $V_{PPL}$ ) 340 $\mu$ s/680 $\mu$ s ( $V_{PPH}$ )	310 $\mu$ s/716 $\mu$ s
	Aligned 64-word Buffered Program Time (typ/max)	-	310 $\mu$ s/900 $\mu$ s
	Aligned 128-word Buffered Program Time (typ/max)	-	375 $\mu$ s/1140 $\mu$ s
	Aligned 256-word Buffered Program Time (typ/max)	-	505 $\mu$ s/1690 $\mu$ s
	Aligned 512-word Buffered Program Time (typ/max)	-	900 $\mu$ s/3016 $\mu$ s
	BEFP Environment Requirement	25 $^{\circ}$ C +/- 5 $^{\circ}$ C 100 P/E cycles	30 $^{\circ}$ C +/- 10 $^{\circ}$ C 50 P/E cycles
	BEFP Setup time	5 $\mu$ s	20 $\mu$ s
	BEFP Time	188KB/s	2.0MB/s
<b>AC characteristics</b>	$t_{DVWH}^{(3)}$	30 ns	30 ns
<b>Erase Performance</b>	Erase Time - 16KW Param. Block (typ/max)	0.4/2.5 s	NA
	Erase Time - 64KW Main Block (typ/max)	0.8/4.0 s	0.8/4.0 s
	Program/Erase Suspend Latency (typ/Max)	20 $\mu$ s/25 $\mu$ s	25 $\mu$ s/30 $\mu$ s
	Blank Check	No	Yes

**Notes:**

1. P30 65nm flash memory device enlarges the program buffer size from 64 Bytes to 1024 Bytes. Optimum programming performance and lower power usage are obtained by aligning the starting address at the beginning of a 512-word boundary (A[9:1] = 0x0000).
2. Program typical speed is improved from 206 KByte/s with 32-word buffer size to 1138 KByte/s with 512-word buffer size.
3. This specification must be complied with by customer's writing timing. Any violation to this timing specification may induce the unpredictable result.

### 5.3 DC Current Specification

The P30 monolithic 65nm device consumes lower power than the P30 stack 130nm device in standby mode.

**Table 5: Key DC Read Specification Comparison**

Features / Specifications		P30 Stack 130nm	P30 Monolithic 65nm
<b>DC Current Characteristics</b>	Standby Current (typ/max)	140/390 $\mu$ A (256-Mbit/ 256-Mbit)	70/225 $\mu$ A (512-Mbit)
	Continuous Burst Read Current (max)	28 mA (52 MHz)	24 mA (52 MHz)
	Program/Erase Current (typ/max)	35/50 mA	35/50 mA
	VPP Factory Program Current (max)	22 mA	Less than 1 mA

## 6.0 Flash Software Design Considerations

The following sections discuss software design considerations when converting from the P30 130nm device to the P30 65nm device.

### 6.1 Device Identification

The P30 130nm stack and P30 65nm monolithic flash devices have different device identification codes. This difference should be addressed during the software update for P30 65nm monolithic flash enabling.

**Table 6: P30 Device ID Codes**

Code Type	Address Offset	Device Density	P30-130nm Stack Codes		P30-65nm Codes		
			Top	Bottom	Uniform	Top	Bottom
Device Identification	0x01	256-Mbit/256-Mbit	8919	891C	-	-	-
		512-Mbit Monolithic	-	-	8999	8960	8961

### 6.2 Read Configuration Register (RCR)(Easy BGA)

Read configurations for both the P30 stack 130nm and P30 monolithic 65nm devices are configured using the Read Configuration Register (RCR). For example, to place the device in synchronous burst-read mode, you set the read mode bit in the RCR.

*Note:* Since the P30 130nm stack flash memory contain two 256-Mbit die, it is necessary to configure the RCR for each die (i.e., twice). Also, it is not possible to do a synchronous burst read across the 256-Mbit die boundary. While the P30 65nm monolithic device is a single die device, the RCR only needs to be configured once, and consequently there is no boundary constraint for synchronous burst read. Software update could utilize this advantage to further improve the performance.

The P30 65nm RCR includes the following modifications to the RCR:

- Latency Count *RCR[14:11]*: an additional bit, RCR14, has been added to the P30 65nm device; RCR14 was reserved on P30 130nm. P30 65nm supports latency counts of 8, 9, 10, 11, 12, 13, 14, and 15.
- WAIT Polarity *RCR[10]*: P30 130nm default setting high and P30 65nm default setting is low.
- Data Hold *RCR[9]*: P30 130nm supports 1-clock or 2-clock cycle data hold configuration. RCR[9] is reserved for P30 65nm and supports a data hold of one cycle only.
- WAIT Delay *RCR[8]*: Same values for P30 130nm and P30 65nm.
- Burst Sequence *RCR[7]*: P30 130nm supports Linear "1" and Intel "0" burst order. P30 65nm supports linear "0" only. Setting P30 65nm to "1" will not affect the burst order; the burst order will always be linear.
- Clock Edge *RCR[6]*: Same values for P30 130nm and P30 65nm.
- Reserved *RCR[5:4]*: Same values for P30 130nm and P30 65nm.
- Burst Wrap *RCR[3]*: Same values for P30 130nm and P30 65nm.
- Burst Length *RCR[2:0]*: Same values for P30 130nm and P30 65nm.

Note: The differences are summarized in the table below.

**Table 7: Read Configuration Register Differences**

Register Field	Value	P30 130nm	P30 65nm
Latency Count	1000 = Code 8 1001 = Code 9 1010 = Code 10 1011 = Code 11 1100 = Code 12	NA	Available
WAIT Polarity	0 = WAIT signal is active low 1 = WAIT signal is active high	Default High	Default Low
Data Hold	0 = Data held for a 1-clock data cycle 1 = Data held for a 2-clock data cycle	Available	1-clock cycle only
Burst Sequence	0 = Reserved 1 = Linear	Intel Burst Order Linear Burst Order	Linear Burst Order, but the default value = 0
Clock Edge	0 = Falling edge 1 = Rising edge	Available	Available
Burst Wrap	0 = Wrap; Burst accesses wrap within burst length set by BL[2:0] 1 = No Wrap; Burst accesses do not wrap within burst length	Available	Available
Burst Length	001 = 4-word burst 010 = 8-word burst 011 = 16-word burst 111 = Continuous-word burst	Available	Available

### 6.3 Blank Check

P30 monolithic 65nm device enables Blank Check function which P30 stack 130nm doesn't. Blank Check is used to confirm whether a main-array block is completely erased. A Blank Check operation is performed one block at a time, and cannot be used during Program Suspend or Erase Suspend.

To use Blank Check, issue the Blank Check setup command then the confirm command. The addressed partition is automatically changed to Read Status Register mode, which remains in effect until another read-mode command is issued. During a blank check operation, the Status Register indicates a busy status (SR7 = 0). Upon completion, the Status Register indicates a ready status (SR7 = 1).

The Status Register should be checked for any errors, and then cleared. If the Blank Check operation fails, which means the block is not completely erased, the Status Register will indicate a Blank Check error (SR[7,5] = 1).

## 6.4 Device Commands

The command set for the P30 monolithic 65nm and P30 stack 130nm devices are fully compatible. However, the P30 65nm device includes new features such as the blank check operation and the enhanced configuration operation. Command set operations are compared here:

**Table 8: Command Bus Operations**

Command		P30 130nm Code (Setup/Confirm)	P30 65nm Code (Setup/Confirm)
Read Modes	Read Array	00FFh	00FFh
	Read Status Register	0070h	0070h
	Clear Status Register	0050h	0050h
	Read Device Information	0090h	0090h
	CFI Query	0098h	0098h
Program/Erase Operations	Word Program	0040h	0040h
	Buffered Program <sup>(1)(2)(3)</sup>	00E8h/00D0h	00E8h/00D0h
	Buffered Enhanced Factory Program	0080h/00D0h	0080h/00D0h
	Block Erase	0020h/00D0h	0020h/00D0h
	Program/Erase Suspend	00B0h	00B0h
	Program/Erase Resume	00D0h	00D0h
	Blank Check	N/A	00BCh/00D0h
Security	Lock Block	0060h/0001h	0060h/0001h
	Unlock Block	0060h/00D0h	0060h/00D0h
	Lock Down Block	0060h/002Fh	0060h/002Fh
	Password Access	N/A	Note 4
Registers	Program Read Configuration Register	0060h/0003h	0060h/0003h
	Program OTP Register	00C0h	00C0h

**Notes:**

1. The device defaults to output SR data after the Buffered Programming Setup Command (E8h) is issued. CE# or OE# must be toggled to update Status Register. Don't issue the Read SR command (70h), which would be interpreted by the internal state machine as Buffer Word Count.
2. During Buffered Program command (E8h) sequence, if a read of the Main Array Data needs to be performed during the loading of the program buffer, then a write to an address outside of current block will abort the Buffer Programming Operation. Issuing the Read Array command (FFh) will put the device into Read Array mode. After Main Array read operation has been completed, the Buffer Program Operation must be restarted.
3. D0h is buffer program confirm command which should be issued at the corresponding block address that the buffer program setup command was issued.
4. Please ask the local representative to get the detail about the password security feature.

## 6.5 WAIT State Comparison

This section will compare the difference between the WAIT states on the P30 stack 130nm and the P30 monolithic 65nm.

### 6.5.1 WAIT State P30 monolithic 65nm

End of wordline (EOWL) WAIT states can result when the starting address of the burst operation is not aligned to a 16-word boundary; that is, A[3:0] of start address does not equal 0x0. Figure 5, "End of Wordline Timing Diagram" on page 16 illustrates the end of wordline WAIT state(s), which occur after the first 16-word boundary is reached. The number of data words and the number of WAIT states for both P30 130nm and P30 65nm are summarized in Table 9, "End of Wordline Data and WAIT State Comparison" on page 16.

Figure 5: End of Wordline Timing Diagram

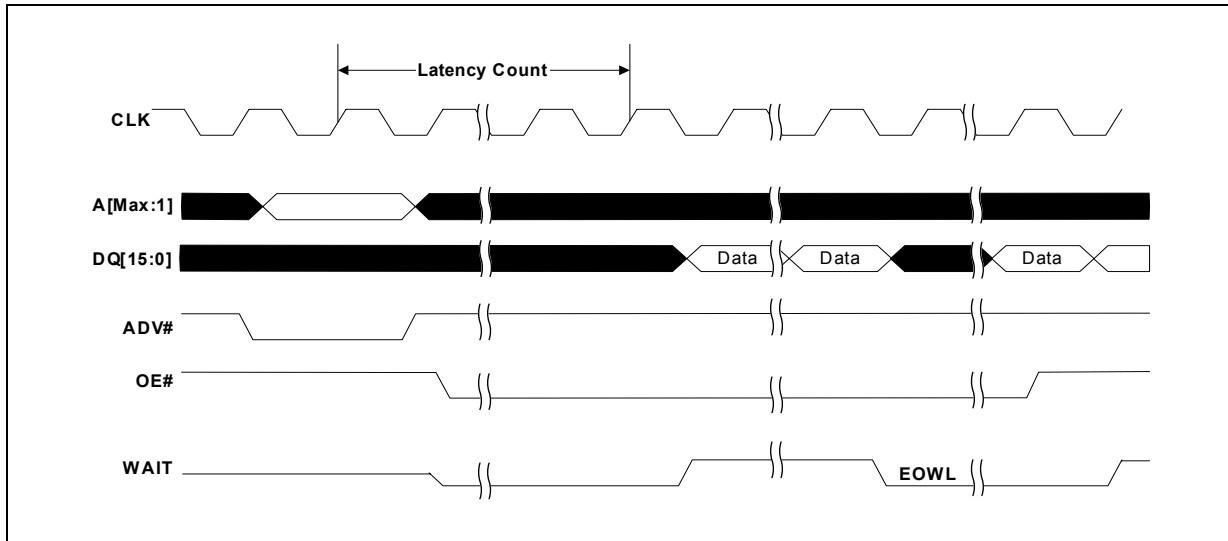


Table 9: End of Wordline Data and WAIT State Comparison

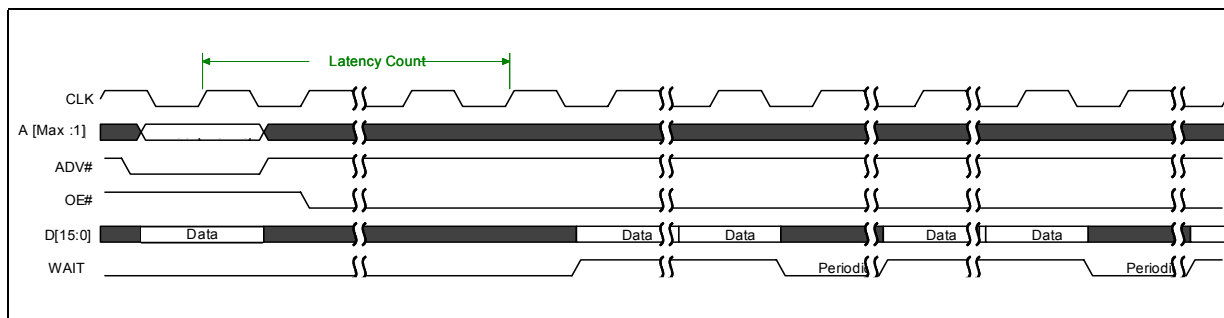
Latency Count	P30 130nm		P30 65nm	
	Data States	WAIT States	Data States	WAIT States
1	Not Supported	Not Supported	Not Supported	Not Supported
2	4	0 to 1	Not Supported	Not Supported
3	4	0 to 2	Not Supported	Not Supported
4	4	0 to 3	Not Supported	Not Supported
5	4	0 to 4	16	0 to 4
6	4	0 to 5	16	0 to 5
7	4	0 to 6	16	0 to 6
8	Not Supported	Not Supported	16	0 to 7
9			16	0 to 8
10			16	0 to 9
11			16	0 to 10
12			16	0 to 11
13			16	0 to 12
14			16	0 to 13
15			16	0 to 14

### 6.5.2 WAIT State P30 Stack 130nm

After encountering an EOWL situation, periodic WAIT states can occur in general as illustrated in Figure 6, "Periodic WAIT State Timing Diagram" on page 17.

Figure 10, "Periodic Data and WAIT State Comparison" on page 17 shows that P30 130nm has periodic WAIT states, but P30 65nm does not.

**Figure 6: Periodic WAIT State Timing Diagram**



**Table 10: Periodic Data and WAIT State Comparison**

Latency Count	P30 130nm		P30 65nm	
	Data States	WAIT States	Data States	WAIT States
1	Not Supported	Not Supported	Not Supported	Not Supported
2	4	0	Not Supported	Not Supported
3	4	0	16	0
4	4	0	16	0
5	4	1	16	0
6	4	2	16	0
7	4	3	16	0
8	Not Supported	Not Supported	16	0
9			16	0
10			16	0
11			16	0
12			16	0
13			16	0
14			16	0
15			16	0

### 6.6 CFI Differences

P30 monolithic 65nm has a different CFI revision. During adoption of Numonyx or third party software, several differences must be taken into account. This section will describe the changes.

### 6.6.1 CFI revision

The CFI minor revision sorted in offset (P+4)h remains as 5.

CFI version 1.5 is supported in the software provided by Numonyx.

### 6.6.2 Time-out changes

All CFI time-out changes are listed in [Table 11, "Value Changes"](#)

**Table 11: Value Changes**

Num	Difference	130nm		65nm	
		offset	value	offset	value
1	"n" such that typical single word program time-out = 2 <sup>n</sup> μ-sec	1Fh	--08	1Fh	--09
2	"n" such that typical max. buffer write time-out = 2 <sup>n</sup> μ-sec	20h	--09	20h	--0A
3	"n" such that maximum word program time-out = 2 <sup>n</sup> times typical	23h	--01	23h	--01
4	"n" such that maximum buffer write time-out = 2 <sup>n</sup> times typical	24h	--01	24h	--02
5	"n" such that maximum number of bytes in write buffer = 2 <sup>n</sup>	2Ah	--06	2Ah	--0A
6	Page Mode Read capability bits 0-7 = "n" such that 2n HEX value represents the number of read-page bytes. See offset 28h for device word width to determine page-mode data output width. 00h indicates no read page buffer.	(P+1D)h	--03	(P+1D)h	--05

### 6.6.3 CFI Link Pointer Removal

P30 130nm stack device has a CFI Pointer, Offset: 112h, DQ7=1, which is used to link to the area offset from 152h to 156h as below [Table 12, "CFI Values Changes"](#). There is no longer a CFI pointer on 65nm 512-Mbit monolithic device and Offset: 112h, DQ7=0. Accordingly, this area offset from 152h to 156h is now in blank.

**Table 12: CFI Values Changes**

Num	Difference	130nm Stack			65nm
		offset	Die 1 (Bot Boot)	Die 2 (Top Boot)	Values
1	CFI Link Field bit definitions				
	Bits 0:9 = Address offset (within 32Mbit segment) of referenced CFI table	152:	--10	--FF	--FF
	Bits 10:27 = nth 32Mbit segment of referenced CFI table	153:	--20	--FF	--FF
	Bits 28:30 = Memory Type	154:	--00	--FF	--FF
	Bit 31 = Another CFI Link field immediately follows	155:	--00	--FF	--FF
2	CFI Link Field Quantity Subfield definitions Bits 3:0 = Quantity field (n such that n+1 equals quantity) Bit 4 = Table & die relative location Bit 5 = Link Field & Table relative location Bits 6:7 = Reserved	156:	--10	--FF	--FF

## 6.7 Performance Improvements in P30 monolithic 65nm

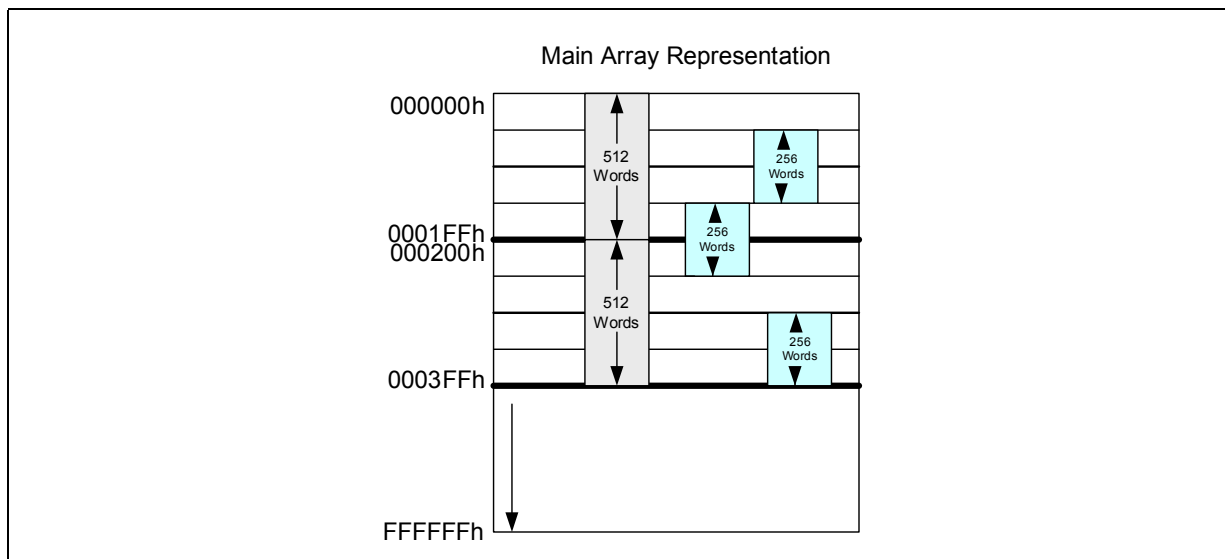
The write performance can be increased on P30 monolithic 65nm by using the 1024 Byte/512 Word buffer. If buffered programming is being done using the 16 word buffer (similar to 130nm devices), no software changes need to be implemented.

To achieve maximum performance using the 1024 Byte/ 512 Word buffer on 65nm devices, the following considerations apply during software modifications:

1. Use the Full 1024 Byte/ 512 Word Buffer
2. If 1024 Byte/ 512 Word Buffer is being used, the programming addresses should be aligned in 512 word address boundaries. For example: Start Programming address is 000000h and End Programming Address is 0001FFh. Please refer to Figure 3.
3. If the addresses must be mis-aligned, they must be in chunks of 256 Words. For example: Start Programming Address to Start Programming Address + 0000FFh (256 Words). Please refer to Figure 3.

The Read performance can be improved by providing read page buffer up to 16 Words (P+1Dh).

**Figure 7: Main Array Representation**



## 7.0 Conversion Considerations

P30 65nm has a larger program buffer size to greatly improve the write performance. Users should use appropriate program and read modes to take advantage of this improved performance.

It is recommended that the user enable robust power loss recovery in software system, especially during the flash write operations. Please refer to the Application Note 309046 for detail information.

## Appendix A Additional Information

Order/Document Number	Document/Tool
306666	Numonyx® Axcell™ Flash Memory (P30-130nm) Datasheet
208042	Numonyx® Axcell™ Flash Memory (P30-65nm) Datasheet
509045	Numonyx® Axcell™ Flash Memory (P30/P33-65nm) Spec Update
309046	Application Note: Power Loss Recovery for Nor Flash Memory

**Note:** Contact your local Numonyx or distribution sales office or visit Numonyx's World Wide Web home page at <http://www.Numonyx.com> for technical documentation, tools, and additional information.