



AN309046

Application Note

How to operate Power Loss Recovery for the
Numonyx™ 65nm Flash Memory Devices

Introduction

This application note describes guidelines on the operations a system designer must perform to recover the flash memory if power loss occurs during a modify operation on Numonyx™ 65nm flash memories' main array.

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1. Flash memory cell structure overview

Numonyx™ 65nm flash memories are based on the leading NOR flash memory products in the embedded market.

Each cell of NOR flash memory resembles a standard MOSFET consisting of two gates: on top is the control gate (CG) and below there is a floating gate (FG) insulated all around by an oxide layer. (See Figure 1: ETOX NOR flash cell structure) When the FG holds a charge, it screens (partially cancels) the electric field from the CG, which modifies the threshold voltage (V_T) of the cell. During read-out, the V_T of the cell is the key factor (given a fixed voltage on CG and Drain) to determine the current flow through the MOSFET channel. The higher the V_T , the smaller the current. By sensing out the current, NOR flash memory generate a binary code accordingly ("0" for small current, "1" for large current). (See Figure 2: V_T based sensing mechanism)

Figure 1: ETOX NOR flash cell structure

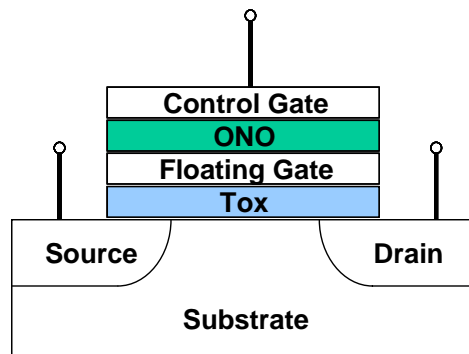
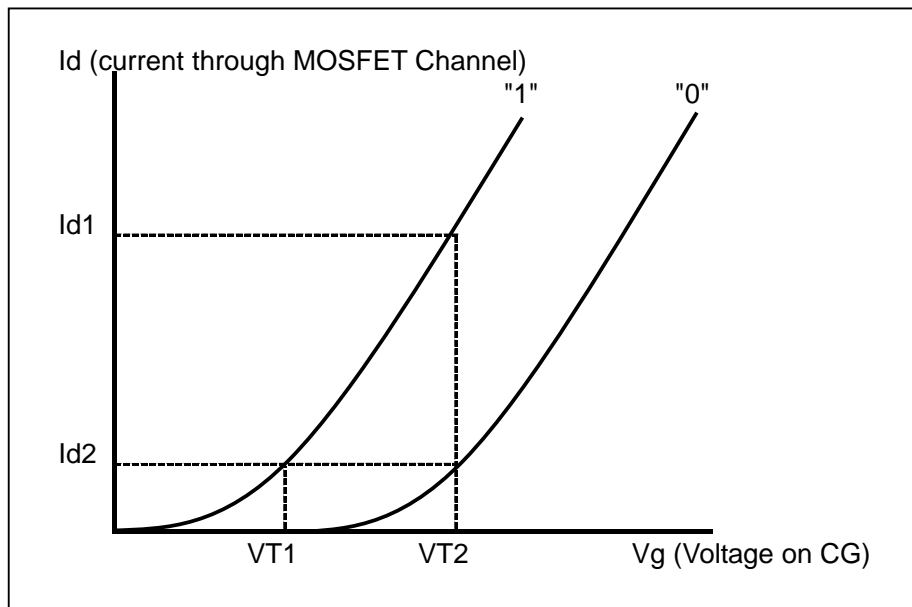


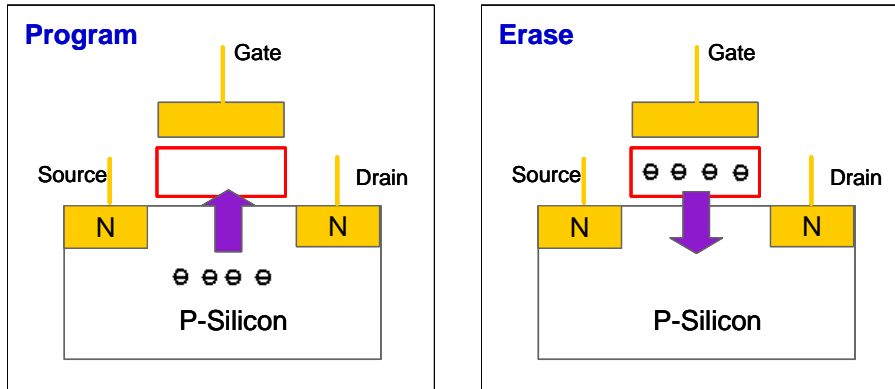
Figure 2: V_T based sensing mechanism



2. Program and Erase mechanism of Flash memory

In general, programming is a process of injecting hot electrons into floating gate and erasing is a process of pulling electrons out of the floating gate. (See Figure 3. Program and Erase mechanism) Both programming and erasing operations require an algorithm which is transparent to users but managed by flash memory itself. This internally controlled algorithm is crucial to make sure proper VT being set for target cells and user see a solid "0" or "1" after a program or erase operation.

Figure 3. Program and Erase mechanism



3. Recovery operations after a power drop

Program and erase operations in flash memory devices take a long time when compared to the average time required by system operations.

During a program or erase operation, a drop in the memory's power supply is possible. In this situation a system designer must know how to recover the memory's status by using the recovery operations shown in Table 1: Recovery operations (please refer to the datasheet for commands not listed).

Without the proper recovery operations (as specified in table 1), system designer faces risk of functional failure due to non-stable flash cell status left over in previous power drop during modify operations.

Table 1. Recovery operations

Before the power drop	To recover
Read operations	
Read Array, Read Electronic Signature, Read Status Register, Read Query	Recovery depends upon the previous status of the flash memory. If the status is in modify, please refer to the modify operation section below.
Clear Status Register	Recovery depends upon the previous status of the flash memory. If the status is in modify, please refer to the modify operation section below.
Modify operations	
Chip/Block Erase	Perform a Chip/Block Erase.
Program Suspend	Program (same address, same data)
Erase Suspend	Erase (same block)
Program Resume	Program (same address, same data)
Erase Resume	Erase (same block)
Unlock Bypass operations	
Unlock Bypass/ Unlock Bypass Reset	No specific recovery instruction is required
Unlock Bypass Program/	Perform the same command(Same address, sameblock) following the right flow to issue it

4. Revision history

Table 2. Document revision history

Date	Revision	Changes
11-Feb-2009	1	Initial release.