



# **Conversion Guide: Numonyx™ StrataFlash® Memory (J3C) to Numonyx™ Embedded Flash Memory (J3 v. D)**

**Application Note - 835**

---

*March 2008*

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH NUMONYX™ PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN NUMONYX'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, NUMONYX ASSUMES NO LIABILITY WHATSOEVER, AND NUMONYX DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF NUMONYX PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. Numonyx products are not intended for use in medical, life saving, life sustaining, critical control or safety systems, or in nuclear facility applications.

Numonyx B.V. may make changes to specifications and product descriptions at any time, without notice.

Numonyx B.V. may have patents or pending patent applications, trademarks, copyrights, or other intellectual property rights that relate to the presented subject matter. The furnishing of documents and other materials and information does not provide any license, express or implied, by estoppel or otherwise, to any such patents, trademarks, copyrights, or other intellectual property rights.

Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Numonyx reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

Contact your local Numonyx sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an order number and are referenced in this document, or other Numonyx literature may be obtained by visiting the Numonyx website at <http://www.numonyx.com>.

Numonyx, the Numonyx logo, and StrataFlash are trademarks or registered trademarks of Numonyx B.V. or its subsidiaries in other countries.

\*Other names and brands may be claimed as the property of others.

Copyright © 2008, Numonyx, B.V., All Rights Reserved.

## Contents

---

<b>1.0</b>	<b>Introduction</b> .....	5
<b>2.0</b>	<b>Conversion from the J3C to the J3 v. D</b> .....	5
2.1	Security Features .....	5
2.2	Block Locking Configuration Read Identification Codes .....	5
2.3	Use of pull-up resistor on VPEN .....	5
<b>A</b>	<b>Specification Changes</b> .....	6
<b>B</b>	<b>Additional Information</b> .....	7

## Revision History

---

Date	Revision	Description
March 2008	001	Initial release

## 1.0 Introduction

This document describes how to convert a system design from the Numonyx™ StrataFlash® Memory (J3) device to the Numonyx™ StrataFlash® Embedded Memory (J3 v. D) device.

## 2.0 Conversion from the J3C to the J3 v. D

The J3 v. D flash memory device is a drop-in compatible replacement for the J3C flash memory device on a smaller 0.13 µm lithography, when the device is used within datasheet specifications. The command set sequences are identical for the J3C and J3 v. D devices, and the pinouts are consistent between new and previous lithographies.

### 2.1 Security Features

The J3 and the J3 v. D devices offer both hardware and software security features. Block lock operations, PRs, and VPEN allow you to implement various levels of data protection. In addition to backward compatibility to its predecessor, J3, the J3 v. D flash memory device offers configurable block locking for enhanced data protection.

For further details regarding J3 v. D security enhancements, see your Numonyx field representative.

### 2.2 Block Locking Configuration Read Identification Codes

When reading the Block Lock Configuration from the data bus on either the J3C or the J3 v. D device, only D[0] is valid. This bit signifies whether the block is unlocked (D0=0) or locked (D0=1). All other bits are invalid (D[7:1] for x8 mode, D[15:1] for x16 mode). When read, these bits return different values for the J3C and J3 v. D devices, as shown in [Table 1](#)

**Table 1: Block Lock Configuration Read Identifier Codes (Hexidecimal)**

Device	Data [15:0] (unlocked)	Data [15:0] (locked)
J3C	FFFC	FFFF
J3 v. D	0000	0001

### 2.3 Use of pull-up resistor on VPEN

Some designs may use a pull-up resistor to put 3.0 V on VPEN. The VPEN pin has a higher current on the J3 v. D device when compared with the J3C during program and erase functions. This is due to process differences (130 nm vs. 180 nm lithography). The voltage drop across the pull-up resistor is too great to drive the correct voltage to the VPEN pin during these functions.

- $I_{ccE/W} \quad V_{cc} = V_{pen} \quad Cmos / TTL \text{ Inputs} \quad I_{ccE/W} = I_{ccE/W} + I_{VpenE/W}$
- Specs for  $I_{ccE/W}$  are 60-80 mA depending on parameters
- Values of  $I_{VpenE/W}$  are 15-100uA depending on lithography (~ 0.2% of overall program or erase current)
- Specs for  $I_{ccE/W}$  remains the same

Numonyx highly recommends that no pull-up resistor to be placed on the VPEN pin; all existing pull-up resistors on J3C must be removed or changed to zero ohm when migrating from the J3C device to the J3 v. D device.

## Appendix A Specification Changes

**Table 2: Timing Specification Changes**

Symbol	Specification	J3A	J3C	J3 v. D	Unit
$t_{AVQV}$	256 Mbit	N/A	125	95	ns
	128 Mbit	150	120	75	ns
	64 Mbit	120	120	75	ns
	32 Mbit	100	115	75	ns
$t_{WHQV3}$ $t_{EHQV3}$	Word Program Typ.	210	210	40	$\mu$ s
	Word Program Max.	630	630	175	$\mu$ s
—	Buffer Program Typ.	218	218	128	$\mu$ s
—	Block Program Time Typ.	0.8	0.8	0.53	s
$t_{WHQV4}$ $t_{EHQV4}$	Block Erase Time Max.	5	5	4	s
$t_{WHQV5}$ $t_{EHQV5}$	Set Lock Bit Time Typ.	64	64	50	$\mu$ s
	Set Lock Bit Time Max.	75	75	60	$\mu$ s
$t_{EHQZ}$	CEx High to Output in High Z	55	35	25	ns
$t_{GLOV}$	OE# to Non-Array Output Delay	30	50	25	ns
$t_{WP}$	Write Pulse Width	70	70	60	ns
$t_{WHRH1}$ $t_{EHRH1}$	Program Suspend Latency Time to Read Typ.	25	25	15	$\mu$ s
	Program Suspend Latency Time to Read Max.	30	75	20	$\mu$ s
$t_{WHRH}$ $t_{EHRH}$	Erase Suspend Latency Time to Read Typ.	26	26	15	$\mu$ s
	Erase Suspend Latency Time to Read Max.	35	35	20	$\mu$ s

## Appendix B Additional Information

Order Number	Document/Tool
290667	Numonyx StrataFlash <sup>®</sup> Memory (J3); 28F128J3, 28F640J3, 28F320J3 Datasheet
298130	Numonyx StrataFlash <sup>®</sup> Memory (J3) 256-Mbit J3 Family Specification Update
298136	Numonyx <sup>®</sup> Persistent Storage Manager User's Guide
292237	AP-689 Using Numonyx <sup>®</sup> Persistent Storage Manager
Note 3	AP-707 3 Volt Numonyx StrataFlash <sup>®</sup> Memory CPU Interface Design Guide
300374	Numonyx StrataFlash <sup>®</sup> Memory J3A to J3C Migration Guide Application Note 792
308551	Numonyx <sup>™</sup> StrataFlash <sup>®</sup> Embedded Memory (J3 v. D) (32, 64, and 128 Mbit) Datasheet
FD	Numonyx <sup>™</sup> StrataFlash <sup>®</sup> Embedded Memory (J3 v. D) (32, 64, 128 and 256 Mbit) Datasheet

**Notes:**

1. Contact your local Numonyx or distribution sales office to request Numonyx documentation..
2. Visit the Numonyx World Wide Web home page at <http://www.Numonyx.com> for further information, technical documentation and tools.

