

Technical Note

Using XIP Modes in the Forte N25Q Flash Memory Device

Introduction

This technical note explains how to implement execute in place (XIP) functionality in an application based on the Micron® Forte™ N25Q Flash memory family. This document does not provide detailed information on the devices but discusses the XIP modes available and highlights the flexibility that XIP offers. For further information, refer to the Ordering Information section of the N25Q device data sheets.

XIP allows software code to execute directly from a long-term storage device, such as nonvolatile memory (Flash) rather than downloading the code and executing it out of a DRAM device.

XIP use in an embedded system provides the benefit of reducing the total amount of memory required, thereby simplifying and reducing the total cost of the system.

Definitions

In this document, the term "XIP mode" means that after the device is selected ($S\# = \text{LOW}$), the memory does not decode the first input byte as command code, but rather as the first part of a 3-byte address. The term "standard mode" means that after the device is selected ($S\# = \text{LOW}$), the memory decodes the first input byte it receives as a command code.

XIP Modes in the N25Q

Micron's N25Q Flash memory family provides a number of XIP modes that can reduce random access time by saving command overhead. The device can be set in XIP mode in any of the following available protocols: extended SPI, DIO-SPI, or QIO-SPI. The number of clock cycles saved depends on the protocol used. The corresponding random access time improvement depends on the operating frequency.

Table 1: Clock Cycles Saved Using XIP Modes

Protocol	Clock Cycles Saved	Random Access Time Improvement (@108 MHz)
Extended SPI	8	74ns
DIO-SPI	4	37ns
QIO-SPI	2	18.5ns

When the memory is in XIP mode, only read, confirm, or exit from XIP mode can be performed. Commands are not decoded from the memory when the device is in XIP mode; therefore, any other operation, such as PROGRAM or ERASE, cannot be performed.

After the device is selected ($S\# = \text{LOW}$) and is in XIP mode, the device decodes the input data it receives as an address.

Depending on the application requirements and memory controller characteristics, five different XIP modes can be selected; the difference among them being the number of pins used to input the address and output the data.

Table 2: XIP Modes

XIP Mode	Address	Data
SIO XIP	x1	x1
DOFR XIP	x1	x2
DIOFR XIP	x2	x2
QOFR XIP	x1	x4
QIOFR XIP	x4	x4

After successful completion of the volatile method operations, the device enters XIP mode. Each XIP mode corresponds to a specific FAST READ command.

Table 3: FAST READ Commands and Corresponding XIP Modes

Protocol	FAST READ Command	XIP Mode Selected
Extended SPI	FAST_READ	SIO XIP
	DOFR	DOFR XIP
	DIOFR	DIOFR XIP
	QOFR	QOFR XIP
	QIOFR	QIOFR XIP
DIO-SPI	DCFR	DIOFR XIP
QIO-SPI	QCFR	QIOFR XIP

Entering XIP Mode: Volatile and Nonvolatile Methods

The N25Q device provides two methods for entering XIP mode: volatile and nonvolatile.

If XIP mode is enabled by means of the volatile method, the device functions in standard mode after a power-off and power-on cycle; therefore, it will decode the first byte it receives as a command code. If XIP mode is enabled by means of the nonvolatile method, the device remains in the selected XIP mode after a power-off and power-on cycle; therefore, it will decode the first three bytes it receives as an address.

Regardless of the method used to enter XIP mode, it is possible to exit XIP mode at any time.

Volatile Method

Micron XIP device: For a Micron XIP device in standard mode, the following operations must be performed to enter XIP mode by the volatile method. The commands are identical regardless of the protocol (extended SPI, DIO-SPI, or QIO-SPI).

1. Enable XIP mode: Perform a WRITE VOLATILE CONFIGURATION REGISTER command to set VCR<3> to 0. This enables the device to enter XIP mode but does not set the specific XIP mode.
2. Set the specific XIP mode: Perform one of the fast read commands in the protocol currently used to set the specific XIP mode:
 - For extended SPI protocol: READ DATA BYTES AT HIGHER SPEED (FAST_READ), DUAL OUTPUT FAST READ (DOFR), DUAL INPUT/OUTPUT FAST READ (DIOFR), QUAD OUTPUT FAST READ (QOFR), OR QUAD INPUT/OUTPUT FAST READ (QIOFR)
 - For DIO-SPI protocol: DUAL COMMAND FAST READ (DCFR)
 - For QIO-SPI protocol: QUAD COMMAND FAST READ (QCFR)
3. Set DQ0: During the first dummy clock cycle after the command code, set DQ0 (XIP confirmation bit) to 0.

After the next deselection and selection cycle, the device will decode the first three bytes it receives as an address.

A Micron XIP device enters QIOFR XIP mode only if VCR<3> has been set to 0 in advance; that is, even if the XIP confirmation bit is set to 0, VCR<3> must be set to 0 in advance. (See Figure 1.)

Basic XIP device: A basic XIP device is always enabled for XIP mode and VCR<3> is always “Don’t Care;” therefore, only the following two commands are required.

1. Set the specific XIP mode: Perform one of the FAST READ commands in the protocol currently used to set the specific XIP mode.
 - For extended SPI protocol: READ DATA BYTES AT HIGHER SPEED (FAST_READ), DUAL OUTPUT FAST READ (DOFR), DUAL INPUT/OUTPUT FAST READ (DIOFR), QUAD OUTPUT FAST READ (QOFR), OR QUAD INPUT/OUTPUT FAST READ (QIOFR)
 - For DIO-SPI protocol: DUAL COMMAND FAST READ (DCFR)
 - For QIO-SPI protocol: QUAD COMMAND FAST READ (QCFR)
2. Set DQ0: During the first dummy clock cycle after the command code, set DQ0 (XIP confirmation bit) to 0.

After the next deselection and selection cycle, the device will decode the first three bytes it receives as an address.

A basic XIP device enters QIOFR XIP mode if the XIP confirmation bit is set to 0. If the XIP confirmation bit is set to 1, the device performs the standard QIOFR command. (See Figure 1.)

Standard Legacy – No XIP Mode

To prevent a Micron XIP device from entering XIP mode, set VCR<3> to 1. If VCR<3> is set to 1, the device will always work in standard mode; confirmation bit Xb is “Don’t Care.” (See Figure 1.)

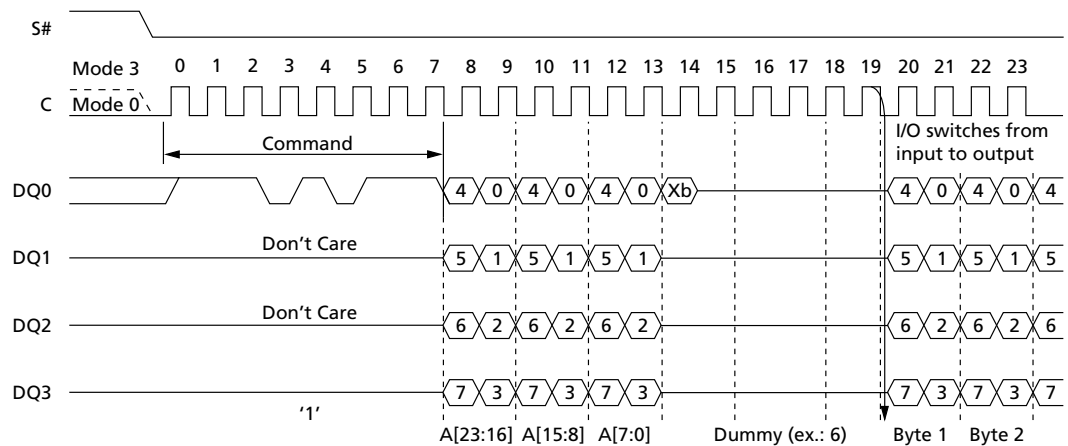
Mixed Working Mode

It is possible to have a basic XIP device that doesn’t enter XIP mode for the FAST_READ and DOFR commands, but it can typically enter XIP mode for DIOFR, QOFR, and QIOFR commands.

Setting the confirmation bit Xb to 1 at the first clock of dummy cycles prevents the device from entering XIP mode; the device will operate in standard mode after the next deselection and selection cycle.

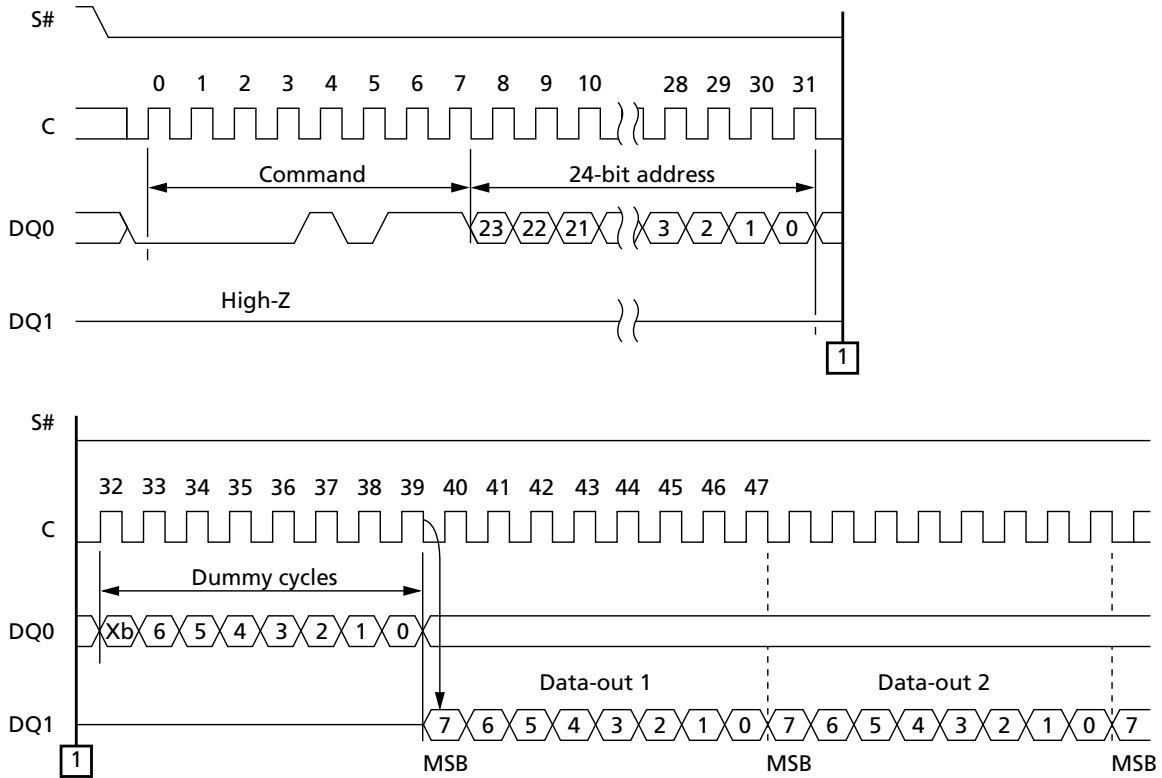
If the XIP confirmation bit is set to 0, the device enters QIOFR XIP mode after the next deselection and selection cycle. If the XIP confirmation bit is set to 1, the device performs the standard QIOFR command after the next deselection and selection cycle.

Figure 1: QIOFR Command



Note: 1. Xb = XIP confirmation bit.

Figure 2: FAST_READ Command



Note: 1. Xb = XIP confirmation bit.

Nonvolatile Method

The nonvolatile method to enter XIP relies on the nonvolatile configuration register (NVCR) to enter XIP mode. This register defines device settings at power-up.

The NVCR bit settings determine the default working behavior of the device after power-on and allow selection of the default working mode, the standard mode, or one of the five XIP modes available.

NVCR is programmable, so it is possible to perform a WRITE NONVOLATILE CONFIGURATION REGISTER command at any time, and thereby change the register's content, provided that the device is not in an XIP mode. When the device is in XIP mode, only READ, CONFIRM, and EXIT XIP STATE commands can be performed.

For a basic XIP device or a Micron XIP device in standard mode, the following commands must be issued to enter XIP mode using the nonvolatile method. Commands are identical for a basic XIP device and a Micron XIP device, regardless of the protocol (extended SPI, DIO-SPI, or QIO-SPI).

1. Perform a WRITE NONVOLATILE CONFIGURATION REGISTER command to set the three XIP bits (11, 10, and 9) to one of the combinations shown in the table below. These three-bit combinations are the available XIP default working mode combinations. The N25Q device is delivered with the default values for these bits (111), corresponding to the standard mode as the default working mode after power-on reset.
2. Perform a power-off and power-on cycle.

After the successful completion of the nonvolatile method command sequence, the device enters the selected XIP working mode according to the particular NVCR XIP bits combination selected.

Table 4: NVCR XIP Bits and Corresponding Default Working Mode

NVCR Bits <11:9>	Default Working Mode After Power-On
000	SIO XIP
001	DOFR XIP
010	DIOFR XIP
011	QOFR XIP
100	QIOFR XIP
111	Standard mode (no XIP)

After performing a WRITE NONVOLATILE CONFIGURATION REGISTER command to set the three XIP bits (11, 10, and 9) to one of the combinations, the device will continue to work in standard mode. It enters the selected XIP mode only after the next power-off and power-on cycle.

Once the NVCR XIP bits are set in a valid XIP default working mode combination, after every subsequent power-on cycle, the device will work in the selected XIP mode unless the NVCR content is changed.

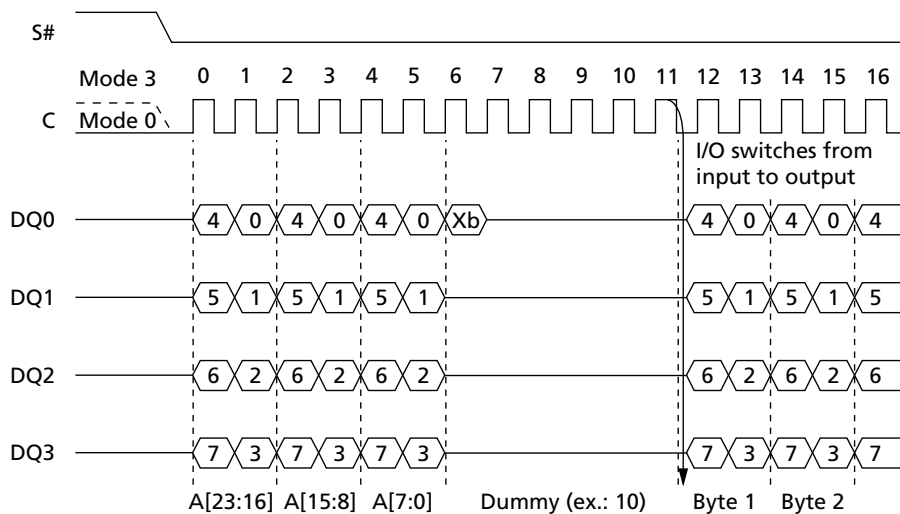
How to Maintain the Memory in XIP Mode

Once in XIP mode, and regardless of how XIP mode was set, the device performs the following sequence when selected:

- Receives as input a 3-byte address
- Waits during dummy clock cycles to perform internal READ operation
- Decodes as XIP confirmation bit the first bit on DQ0 during the first dummy clock cycles
- Outputs the data (starting from the addressed byte) in sequence until it is again deselected (S# = HIGH)

To hold the memory in the selected XIP mode, the XIP confirmation bit must be set to 0.

Figure 3: QIOFR XIP Mode



Note: 1. Xb = XIP confirmation bit.

Exiting XIP Mode

The standard method of exiting XIP mode is to set the XIP confirmation bit to 1 during the first dummy clock cycle after the address. After the next deselection and selection cycle, the memory starts working in standard mode, accepting commands and not directly addresses. If the XIP mode has been set by the volatile method, a power-off and power-on cycle also sets the memory in standard mode.

For devices with reset pin functionality (those which have not had this functionally disabled), setting RESET# LOW also returns the device to standard mode, provided that the XIP bits of the NVCR (11, 10, and 9) equal 111.

For devices without the reset pin functionality, a particular sequence can be implemented in the memory controller software to prevent the memory controller hardware from being reset (or accidentally powered off) while the memory is in XIP mode. In this case, the standard boot sequence of the memory controller would not work because the memory would decode any input byte as part of an address and not as a command. The recommended rescue sequence for this case is described in the N25Q device data sheets.

Conclusion

Micron's N25Q devices can be set in five different XIP modes to fit specific application requirements and performance needs. XIP mode reduces memory random access time by saving clock cycle overhead. This performance enhancement is useful in XIP applications because the code can be directly executed on the SPI Flash without having to be downloaded to a DRAM device. The N25Q provides two methods for entering XIP mode:

- Volatile method, recommended for applications that boot with the memory in standard mode
- Nonvolatile method, recommended for applications that boot directly with the memory in the required XIP mode

The N25Q Flash memory family is the first quad I/O solution in the market to offer both of these options.



Revision History

Rev. B – 2/11

- Conversion

Rev. 01 – 10/09

- Initial release

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