
**How to migrate from
M29DW128FH/L to M29DW128GH/L Flash memories**

Introduction

The objective of this application note is to explain how to migrate an application based on the M29DW128FH/L Flash memory to an M29DW128GH/L Flash memory. The purpose of this document is not to provide detailed information on the devices, but to highlight the similarities and differences between them. The comparison takes into consideration the signal descriptions, packages, architecture, software command set, performance, and block protections.

The M29DW128FH/L and M29DW128GH/L are 128 Mbit (8 Mb x 16 or 16 Mb x 8) Flash memories that can be read, erased and reprogrammed using a single low supply voltage. Both memories are divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.

Further M29DW128FH/L and M29DW128GH/L are divided into four banks, A, B, C and D, providing multiple bank operations. While programming or erasing in one bank, read operations are possible in any other bank.

Program and Erase commands are written to the command interface of the memory. An on-chip Program/Erase controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents.

A group of blocks can be protected to prevent accidental Program or Erase commands from modifying the memory. On both devices, the highest or lowest memory block can also be protected by using a hardware method.

All devices have an extra block, the extended block, of 128 words (256 bytes). It can be accessed using a dedicated command. The extended block can be protected and so is useful for storing security information. However the protection is not reversible; once protection is enabled, it cannot be undone.

The M29DW128FH (highest block protected) and M29DW128FL (lowest block protected) will be referred to as M29DW128F.

The M29DW128GH (highest block protected) and the M29DW128GL (lowest block protected) will be referred to as M29DW128G.

Please refer to the M29DW128F and M29DW128G datasheets for additional information on devices.

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1 Memory architecture and protection groups

The M29DW128F and the M29DW128G memory arrays are divided into asymmetrical blocks. The M29DW128F features 16 parameter and 254 main blocks, while the M29DW128G features 8 parameter and 62 main blocks.

Both arrays memory are divided into four banks, A, B, C and D, providing multiple bank operations. While programming or erasing in one bank, read operations are possible in any other bank.

The M29DW128F has 16 parameter blocks of 4Kwords/8Kbytes, eight of the Parameter Blocks are at the top of the memory address space, and eight are at the bottom; while the M29DW128G has 8 parameter blocks of 32Kwords/64Kbytes, four of the parameter blocks are at the top of the memory address space, and four are at the bottom. The bank architecture is summarized in [Table 1: Memory organization](#).

The M29DW128F has a 128-Word/256-Byte extended memory block, with 64 Words/128 Bytes Factory Locked, and 64 Words/128 Bytes Customer Lockable. The M29DW128G has a bigger Extended Memory block with 256 Words, divided in 128 Words Factory Locked and 128 Words Customer Lockable. See [Section 3: Software command set on page 11](#) for a description of the extended memory block commands.

Another difference between the M29DW128F and the M29DW128G is protection groups:

- On the M29DW128F, all the parameter blocks are protected individually. Blocks 8,9 and 10 are grouped in a single protection block. Blocks 256, 257, 258 are grouped in a single protection block. All the other blocks are grouped by four.
- On the M29DW128G, all blocks are protected individually. The protection granularity is always 64Kwords or 128Kbytes on the M29DW128G.

Table 1 Memory organization

| | M29DW128F | M29DW128G |
|------------------------|--|--|
| Banks organization | 16 Mbit / 48 Mbit / 48 Mbit / 16 Mbit | 16 Mbit / 48 Mbit / 48 Mbit / 16 Mbit |
| Parameter organization | Bank A and Bank D have 8 parameter blocks of 4 KWords / 8 KBytes | Bank A and Bank D have 4 parameter blocks of 32 KWords / 64 KBytes |
| Block size | 32 KWords / 64 KBytes | 128 KWords / 256 KBytes |

2 Hardware migration

This section provides a detailed comparison between M29DW128F and M29DW128G signals and package pin-out.

2.1 Signal description

[Table 2: Comparison: signal description for M29DW128F and M29DW128G devices](#) gives a comparison between the M29DW128F and M29DW128G signals. The devices are compatible except for the VCCQ signal, BYTE signal and a few slight differences in the VPP/WP signal and RP signal.

2.1.1 VCCQ Pin

In the M29DW128G devices, VCCQ provides the power supply to the I/O pins and enable all outputs to be powered independently from VCC. This is an added feature which is not present in the M29DW128F devices. However, the M29DW128G devices are compatible with all the applications using the M29DW128F devices even if they feature the VCC supply voltage only.

2.1.2 BYTE pin

M29DW128F differs from M29DW128G for BYTE pin only present in the TSOP package. In the same position of M29DW128F BYTE pin, in M29DW128G TSOP package there is a not connected pin, this pin can be leave connected to VCC, to VSS or not connected.

2.1.3 VPP/WP Pin

On both devices, the VPP function allows the memory to use an external high voltage power supply to reduce the time required for Fast Program operations. The Write Protect (WP) function provides a hardware method of protecting the outermost memory block:

- When (VPP/WP) is Low, VIL, the highest or lowest block is protected on both the M29DW128G and M29DW128F devices. In M29DW128F, program and erase operations in this block are ignored while VPP/WP is Low, even when RESET (RP) is at VID (temporary no protection).
- When VPP/WP is High, VIH, the memory reverts to the previous protection status of the outermost block.

On the M29DW128F devices, applying 12 V to the VPP/WP pin will temporarily unprotect any block previously protected (including the two outermost blocks). On the M29DW128G devices this functionality is available upon customer request. In addition, the VPP/WP pin must not be left floating or unconnected on the M29DW128F, whereas M29DW128G VPP/WP is High, VIH, when unconnected, due to an internal pull-up.

2.1.4 RP PIN

On both devices, the Reset is used to apply a Hardware Reset to the memory by holding a low, VIL, for at least tPLPX, while only in M29DW128F RP can be used also to temporarily unprotect all the blocks previously protected using a High Voltage Block Protection technique (In-System or Programmer technique).

Table 2 Comparison: signal description for M29DW128F and M29DW128G devices

| Name | Description | Direction | M29DW128F | M29DW128G |
|------------------------|------------------------------------|-----------|-------------------------------------|---|
| A0-A22 | Address inputs | Inputs | — | — |
| DQ0-DQ7 | Data inputs/outputs | I/O | — | — |
| DQ8-DQ14 | Data inputs/outputs | I/O | — | |
| DQ15A-1 | Data input/output or address input | I/O | — | DQ15 only / x8 mode not available |
| \overline{E} | Chip Enable | Input | — | |
| \overline{G} | Output Enable | Input | — | |
| \overline{W} | Write Enable | Input | | |
| \overline{RP} | Reset | Input | Reset and block temporary unprotect | |
| \overline{RB} | Ready/Busy output | Output | — | |
| \overline{BYTE} | Byte/word organization select | Input | — | Not available / x16 only |
| V_{CC} | Supply voltage | Supply | — | |
| V_{CCQ} | I/O buffer supply voltage | Supply | Not available | |
| V_{PP}/\overline{WP} | V_{PP} /Write Protect | Input | — | V_{PP}/\overline{WP} may be left floating since it is internally connected to a pull-up resistor which enables program/erase operations |
| V_{SS} | Ground | - | — | — |
| NC | Not connected internally | - | — | — |

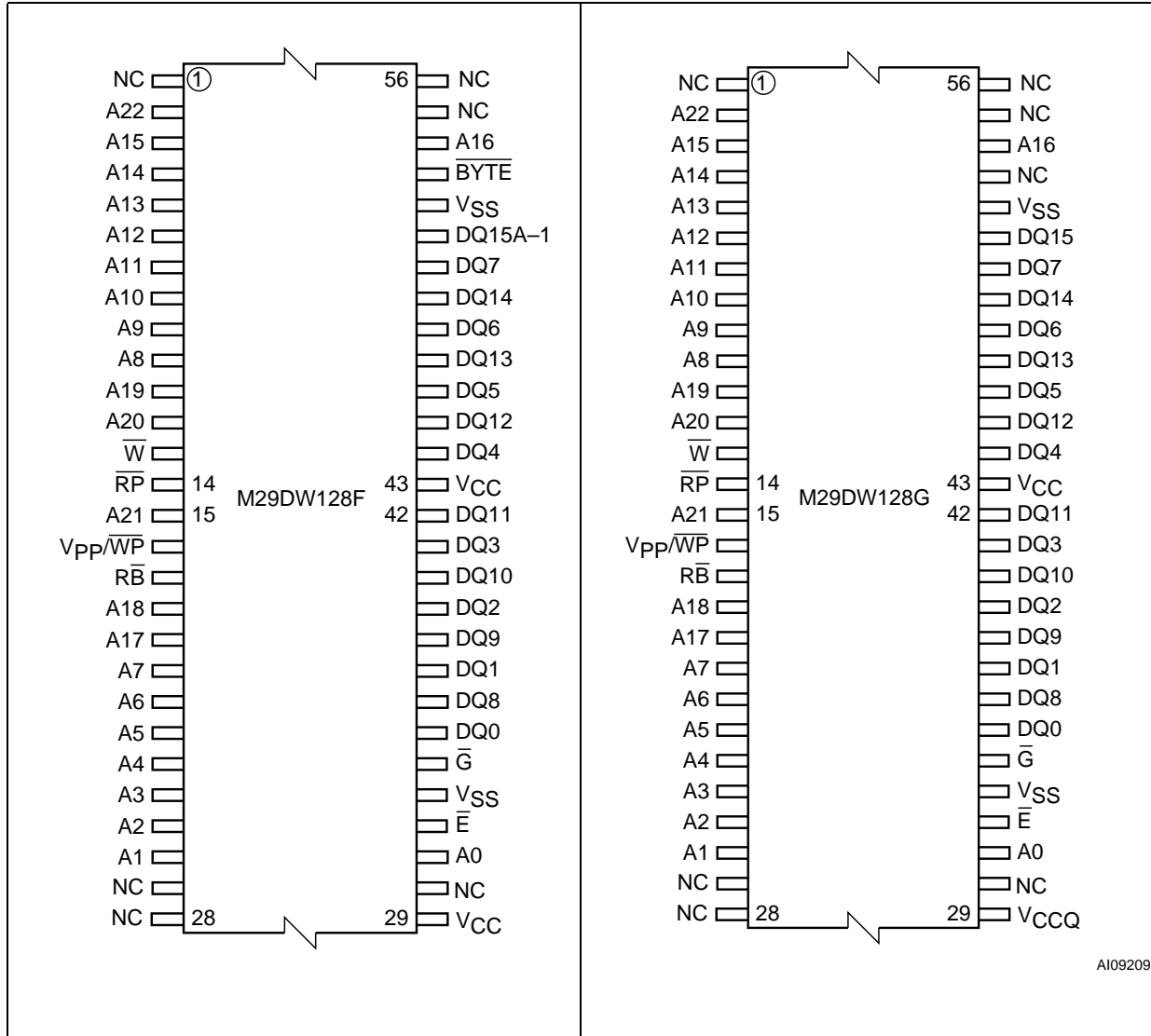
2.2 Packages

The M29DW128F and M29DW128G are delivered in TSOP56 - 14 x 20 mm, and TBGA64 - 10 x 13 mm, 1 mm pitch packages.

The M29DW128G is fully pin-to-pin compatible, except for BYTE pin (x8 mode), with the M29DW128F (the vice versa is not true due to the VCCQ pin). Pin connections for TSOP and Ball connection for TBGA are shown here. See also [Table 2: Comparison: signal description for M29DW128F and M29DW128G devices](#).

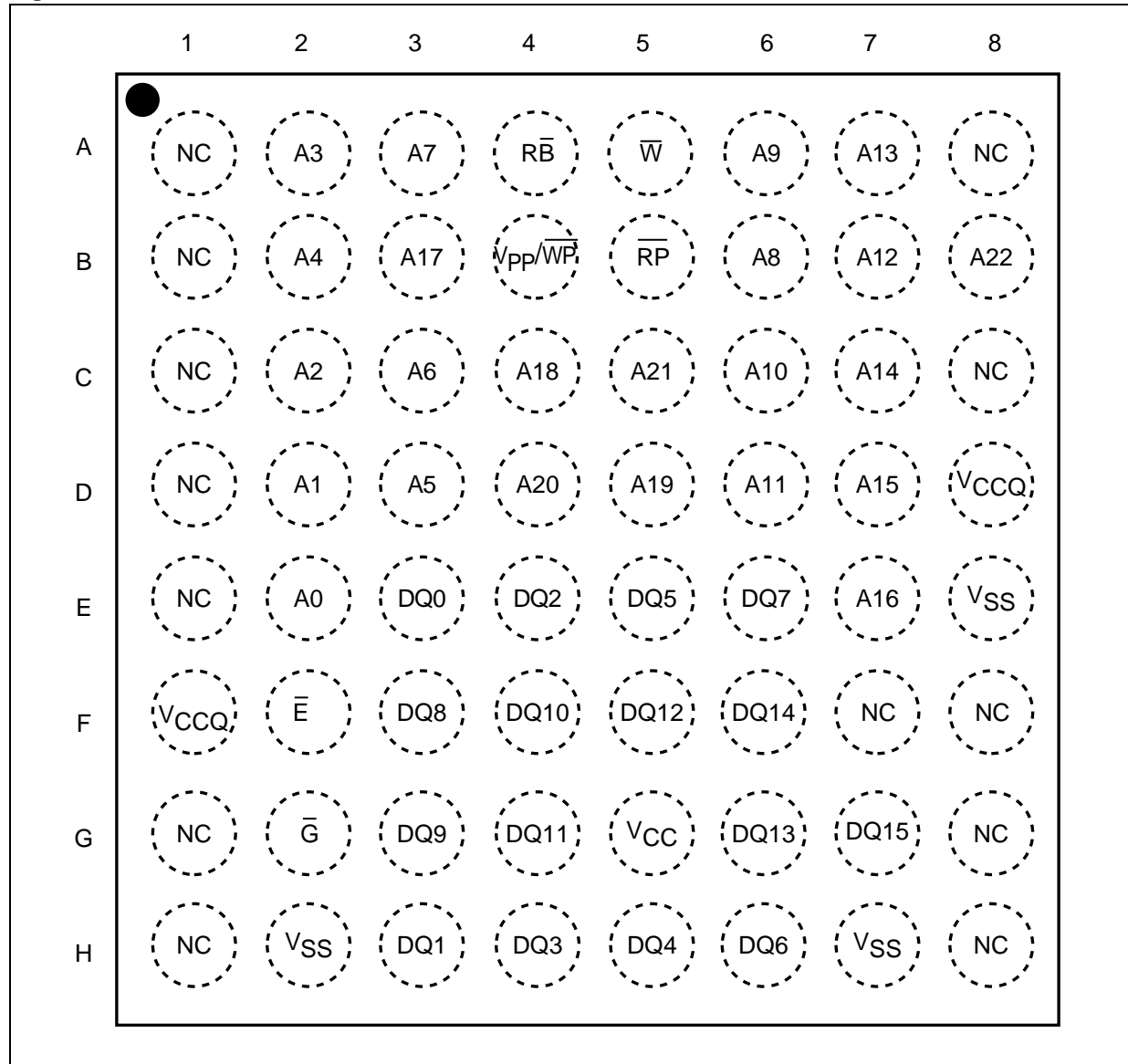
Note: Refer to the M29DW128F and M29DW128G datasheets for details on the packages.

Figure 1 M29DW128F TSOP56 connections **Figure 2 M29DW128G TSOP56 connections**



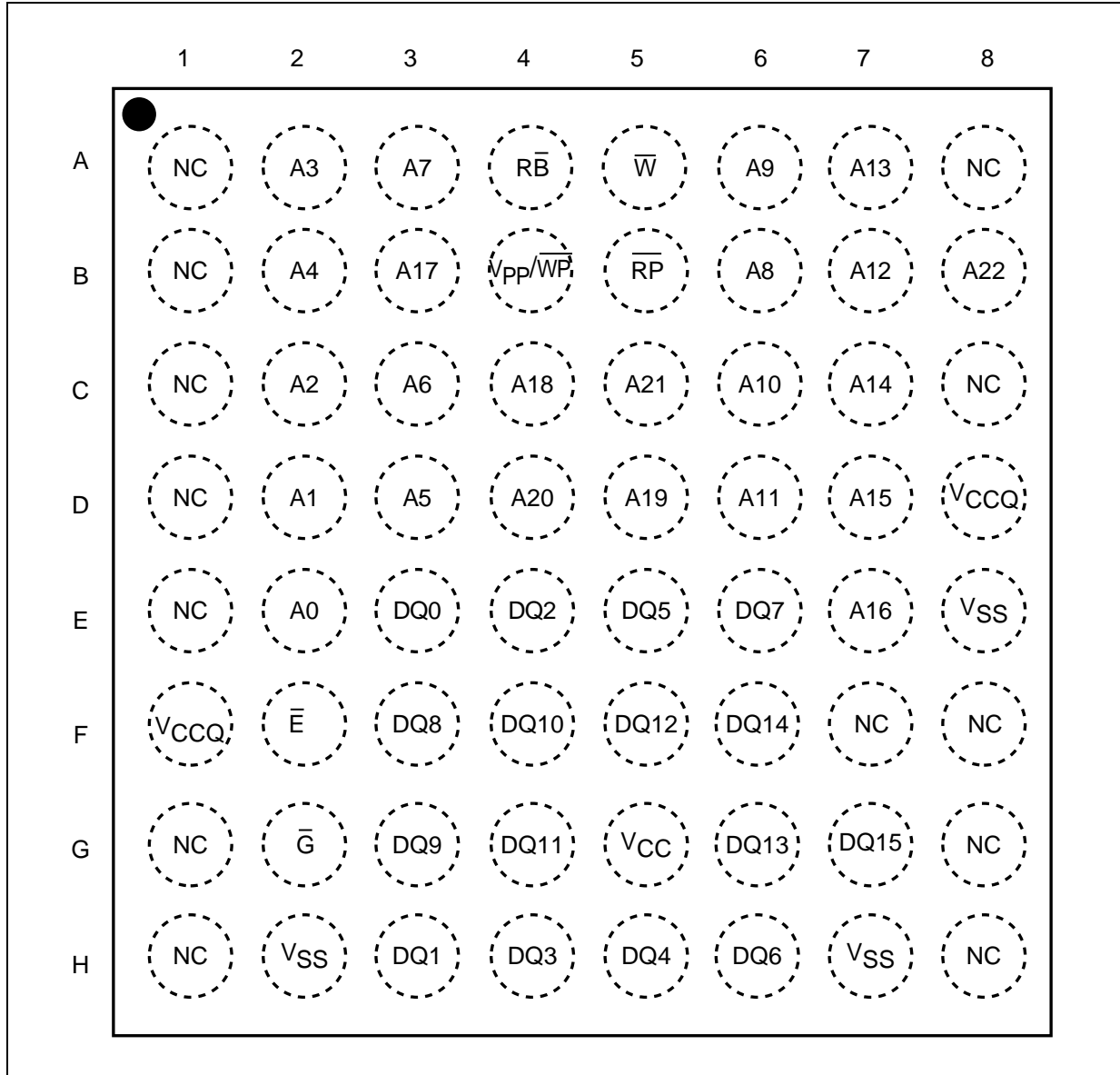
AI09209

Figure 3 M29DW128F TBGA64 connections



Note: *BYTE pin not present in this package.*

Figure 4 M29DW128G TBGA64 connections



3 Software command set

The M29DW128F and M29DW128G feature an identical set of standard commands. The commands are compliant with the JEDEC standard.

The only difference is related to 0xFF command. M29DW128G doesn't tolerate 0xFF as a valid command, and once 0xFF is issued to the device, like in some system, the M29DW128G will enter unexpected state. Adding a 0xF0 command systematically after 0xFF command is necessary.

M29DW128F device tolerates 0xFF command. Nothing will happen if it is issued 0xFF command.

3.1 Fast Program commands

The M29DW128F and the M29DW128G devices both feature Fast Program commands.

The Enhanced Buffered Program command is only available on M29DW128G devices. It makes use of the device's 256-word write buffer to speed up programming. To use the Enhanced Buffered Program command, all the 256 words must be loaded into the write buffer in an increasing address order. Each write buffer has the same A22-A8 addresses. The Enhanced Buffered Program command dramatically reduces system programming time.

Double, Quadruple, and Octuple Byte, Double and Quadruple Word Program commands are only available on M29DW128F devices.

In M29DW128G devices it is recommended to use Enhanced Buffered Program and Write to Buffer Program commands to reach the best programming speed. In addition, the M29DW128G devices feature a full set of Unlock Bypass commands as shown in the tables here.

Table 3 Enhanced Buffered Program commands, M29DW128G⁽¹⁾⁽²⁾

| Command | Length | Bus write operations | | | | | | | | | | | | | | | | | |
|---|--------|----------------------|------|----------|------|-----|------|----------|------|-----|------|----------|------|-------|------|----------|------|-------|------|
| | | 1st | | 2nd | | 3rd | | 4th | | ... | | 257th | | 258th | | 259th | | 260th | |
| | | Add | Data | Add | Data | Add | Data | Add | Data | Add | Data | Add | Data | Add | Data | Add | Data | Add | Data |
| Enhanced Buffered Program | 259 | 555 | AA | 2AA | 55 | BAd | 33 | BAd (00) | Data | ... | ... | | | | | BAd (FF) | Data | | |
| Enhanced Buffered Program Confirm | 1 | BAd (00) | 29 | | | | | | | | | | | | | | | | |
| Unlock Bypass Enhanced Buffered Program | 257 | BAd | 33 | BAd (00) | Data | | | | | | | BAd (FF) | Data | | | | | | |

1. Only available from week 8 of 2008.
2. BAd any address in the block.

Table 4 Fast program commands, M29DW128G

| Command | Length | Bus write operations ⁽¹⁾ | | | | | | | | | | | |
|---------------------------------------|--------|-------------------------------------|------|-----|------------------|-------------------|------|--------------------|------------------|-------------------|------|--------------------|------|
| | | 1st | | 2nd | | 3rd | | 4th | | 5th | | 6th | |
| | | Add | Data | Add | Data | Add | Data | Add | Data | Add | Data | Add | Data |
| Write to Buffer Program | N+5 | 555 | AA | 2AA | 55 | BAd | 25 | BAd | N ⁽²⁾ | PA ⁽³⁾ | PD | WBL ⁽⁴⁾ | PD |
| Write to Buffer Program Confirm | 1 | BAd ⁽⁵⁾ | 29 | | | | | | | | | | |
| Buffered Program Abort and Reset | 3 | 555 | AA | 2AA | 55 | 555 | F0 | | | | | | |
| Unlock Bypass | 3 | 555 | AA | 2AA | 55 | 555 | 20 | | | | | | |
| Unlock Bypass Program | 2 | X | A0 | PA | PD | | | | | | | | |
| Unlock Bypass Block Erase | 2+ | X | 80 | BAd | 30 | | | | | | | | |
| Unlock Bypass Chip Erase | 2 | X | 80 | X | 10 | | | | | | | | |
| Unlock Bypass Write to Buffer Program | N+3 | BAd | 25 | BAd | N ⁽²⁾ | PA ⁽³⁾ | PD | WBL ⁽⁴⁾ | PD | | | | |
| Unlock Bypass CFI | 1 | BKA | 98 | | | | | | | | | | |
| Unlock Bypass Reset | 2 | X | 90 | X | 00 | | | | | | | | |

1. X don't care, PA program address, PD program data, BAd any address in the block, BKA bank address, WBL write buffer location. All values in the table are in hexadecimal.
2. The maximum number of cycles in the command sequence is 36. N+1 is the number of words to be programmed during the write to buffer program operation.
3. Each buffer has the same A22-A5 addresses. A0-A4 are used to select a word within the N+1 word page.
4. The 6th cycle has to be issued N time. WBL scans the word inside the page.
5. BAd must be identical to the address loaded during the write to buffer program 3rd and 4th cycles.

Table 5 Fast Program Commands, 16-bit mode⁽¹⁾, M29DW128F

| Command | Length | Bus Write operations | | | | | | | | | | | |
|---|--------|----------------------|------|-----|------|-----|------|-----|------------------|-------------------|------|--------------------|------|
| | | 1st | | 2nd | | 3rd | | 4th | | 5th | | 6th | |
| | | Add | Data | Add | Data | Add | Data | Add | Data | Add | Data | Add | Data |
| Write to Buffer and Program | N+5 | 555 | AA | 2AA | 55 | BA | 25 | BA | N ⁽²⁾ | PA ⁽³⁾ | PD | WBL ⁽⁴⁾ | PD |
| Write to Buffer and Program Abort and Reset | 3 | 555 | AA | 2AA | 55 | 555 | F0 | | | | | | |
| Write to Buffer and Program Confirm | 1 | BA ⁽⁵⁾ | 29 | | | | | | | | | | |
| Double Word Program | 3 | 555 | 50 | PA0 | PD0 | PA1 | PD1 | | | | | | |
| Quadruple Word Program | 5 | 555 | 56 | PA0 | PD0 | PA1 | PD1 | PA2 | PD2 | PA3 | PD3 | | |

Table 5 Fast Program Commands, 16-bit mode⁽¹⁾, M29DW128F

| Command | Length | Bus Write operations | | | | | | | | | | | |
|-----------------------|--------|----------------------|------|-----|------|-----|------|-----|------|-----|------|-----|------|
| | | 1st | | 2nd | | 3rd | | 4th | | 5th | | 6th | |
| | | Add | Data | Add | Data | Add | Data | Add | Data | Add | Data | Add | Data |
| Unlock Bypass | 3 | 555 | AA | 2AA | 55 | 555 | 20 | | | | | | |
| Unlock Bypass Program | 2 | X | A0 | PA | PD | | | | | | | | |
| Unlock Bypass Reset | 2 | X | 90 | X | 00 | | | | | | | | |

1. X Don't Care, PA Program Address, PD Program Data, BA Any address in the Block, BKA Bank Address, WBL Write Buffer Location. All values in the table are in hexadecimal.
2. The maximum number of cycles in the command sequence is 36. N+1 is the number of Words to be programmed during the Write to Buffer and Program operation.
3. Each buffer has the same A5-A22 addresses. A0-A4 are used to select a Word within the N+1 Word page.
4. The 6th cycle has to be issued N time. WBL scans the Word inside the page.
5. BA must be identical to the address loaded during the Write to buffer and Program 3rd and 4th cycles.

3.2 Program operation fails detection

In M29DW128G devices, it is possible to detect Program operation fails, even during a Write to Buffer or Enhanced Buffered Program, when changing programmed data from '0' to '1', that is when reprogramming data in a portion of memory already programmed. The resulting data will be the logical OR between the previous value and the current value.

In M29DW128F devices, this functionality is not available for the Write to Buffer command.

3.3 Device codes and auto select codes

The auto select codes are composed of the manufacturer code, the device code, the block protection status, and the extended memory block verify code.

The M29DW128F and M29DW128G devices have the same manufacturer code but different device code and extended memory block verify code.

The M29DW128F and M29DW128G devices use identical commands and address inputs to read the auto select codes.

Table 6 Root part number and device code

| Root part number | Device code |
|------------------|-----------------------|
| M29DW128F | 227Eh + 2220h + 2200h |
| M29DW128G | 227Eh+2220h+2202h |

Table 7 Block Protection, 16-bit mode⁽¹⁾, M29DW128F

| Operation | \bar{E} | G | \bar{W} | \bar{RP} | V _{PP} /WP | Address Inputs | | | | | | | | Data Inputs/Outputs | | |
|---|-----------------|-----------------|-----------------|-----------------|---------------------|----------------|---------|-----------------|-----------------|----|-----------------|-------|-----------------|---------------------|-----------------|---|
| | | | | | | A22-A12 | A11-A10 | A9 | A8 | A7 | A6 | A5-A4 | A3-A2 | A1 | A0 | DQ15A-1, DQ14-DQ0 |
| Verify Extended Block Indicator (bits DQ6, DQ7) | V _{IL} | V _{IL} | V _{IH} | V _{IH} | V _{IH} | BA | X | V _{ID} | X | X | V _{IL} | X | V _{IL} | V _{IH} | V _{IH} | 0080h (Customer Lockable) 00C0h (Customer Locked) ⁽²⁾ |
| Verify Block Protection Status | | | | | | BKA | | | V _{IL} | | V _{IL} | | | V _{IL} | | 0001h (protected) 0000h (unprotected) |
| Temporary Block Unprotect ⁽³⁾ | X | X | X | V _{ID} | X | Valid | | | | | | | | Data Input | | |

1. X = V_{IL} or V_{IH}. BKA Bank Address, BA Any Address in the Block.
2. This indicates the protection status of the second section of the Extended Block; the first section of the Extended Block being always Factory Locked.
3. The \bar{RP} pin disables protection on all the blocks that have been previously protected using a High Voltage protection Technique.

Table 8 Block protection, 16-bit mode, M29DW128G

| Operation (1) | \bar{E} | \bar{G} | \bar{W} | \bar{RP} | $\frac{V_{PP}}{WP}$ | Address inputs | | | | | | | | | | Data inputs/outputs | | |
|--|-----------|-----------|-----------|------------|---------------------|----------------|---------|----|----|----|----|-------|-------|----|----|---------------------|----------|---|
| | | | | | | A22-A12 | A11-A10 | A9 | A8 | A7 | A6 | A5-A4 | A3-A2 | A1 | A0 | DQ15-DQ0 | | |
| Verify extended memory block indicator bit | V_{IL} | V_{IL} | V_{IH} | V_{IH} | V_{IH} | BKA | | | | | | | | | | | V_{IH} | DQ15-DQ8=0 DQ7: 1=factory locked DQ6: 1=customer locked, 0=customer lockable DQ5: 1=reserved, 0=standard DQ4, DQ3-Hardware write protection: 00= \bar{WP} protects 4 outermost blocks, 11=No \bar{WP} protection DQ2-DQ0=0 |
| Verify block protection status | | | | | | BAd | | | | | | | | | | | V_{IL} | 0000h (unprotected) 0001h (protected) |

1. X = V_{IL} or V_{IH} . BAd any address in the block, BKA bank address.

4 Performance and characteristics

The M29DW128F and the M29DW128G have almost compatible DC and AC characteristics (see the respective datasheets for details). The differences lie in access times, fast programming times, and supply voltages.

4.1 Power Supply

M29DW128G differs from M29DW128F in terms power supply for voltage levels VPPH and VID.

Another feature which is not present in the M29DW128F devices is the presence VCCQ pin; VCCQ pin provides the power supply to the I/O pins and enable all outputs to be powered independently from VCC.

Table 9 Power Supply Comparison

| | M29DW128G | M29DW128F |
|------|------------------|------------------|
| VCC | 2.7 - 3.6 V | 2.7 - 3.6 V |
| VCCQ | 1.65 - 3.6 V | NA |
| VID | 8.5 - 9.5 V | 11.5 - 12.5 V |
| VPPH | 8.5 - 9.5 V | 11.5 - 12.5 V |

4.2 Access time

The M29DW128G has a random access time of 60/70 ns with VCCQ in the range 2.7-3.6V or 80 ns, with the extended VCCQ range 1.65-3.6V, whereas the M29DW128F has an access time of 60 or 70 ns.

4.3 Page Read mode

The Page mode is available on the M29DW128F and M29DW128G to speed up read operations. The data is internally read and stored in a 8-word page buffer.

Using Page read, the access time for subsequent read operations is reduced to 25 ns for both devices with $V_{CCQ}=V_{CC}$, while it is reduced to 30 ns for the M29DW128G with $V_{CCQ} = 1.65$ V.

4.4 Program and Erase times

The time required to program or erase the whole memory is lower on the M29DW128G compared to the M29DW128F. The memory can be programmed by using a Fast Program or an Enhanced Buffered Program command, or by using the word by word program command.

Note: Typical values measured at room temperature and nominal voltages. Except for Program/Erase cycles and Data retention, all values are sampled, but not 100% tested.

Table 10 Program and Erase Times

| Parameter | M29DW128G | | | M29DW128F | | | Unit |
|--|-----------|-----|--------------------|-----------|-----|--------------------|--------|
| | Min | Typ | Max | Min | Typ | Max | |
| Chip Erase | — | 40 | 400 ⁽¹⁾ | — | 80 | 400 ⁽¹⁾ | s |
| Block Erase ⁽²⁾ | — | 1 | — | — | 0.8 | — | s |
| Erase Suspend latency time | — | 25 | 35 | — | — | 50 ⁽¹⁾ | µs |
| Word Program: Single Word | — | 16 | 200 ⁽¹⁾ | — | 10 | 200 | µs |
| Word Program: Write to Buffer (32 words): VPP/WP = VPPH | — | 51 | 200 ⁽¹⁾ | — | 90 | 700 | µs |
| Word Program: Write to Buffer (32 words): VPP/WP = VIH | — | 78 | 200 ⁽¹⁾ | — | 280 | 1400 | µs |
| Chip Program (word by word) | — | 135 | 400 ⁽¹⁾ | — | 40 | 200 ⁽¹⁾ | s |
| Chip Program (Write to Buffer Program) ⁽³⁾ | — | 20 | 200 ⁽¹⁾ | — | 73 | 350 ⁽¹⁾ | s |
| Chip Program (Write to Buffer Program with VPP/WP = VPPH) ⁽³⁾ | — | 13 | 50 ⁽¹⁾ | — | 23 | 180 ⁽¹⁾ | s |
| Faster Chip Program ⁽⁴⁾ | — | 5 | 25 | — | 10 | 50 | s |
| Program Suspend latency time | — | 5 | 15 | — | 5 | 15 | µs |
| Program/Erase cycles (per block) | 100,000 | — | — | 100,000 | — | — | Cycles |
| Data retention | 20 | — | — | 20 | — | — | Years |

1. *Maximum value measured at worst case conditions for both temperature and VCC after 100,000 program/erase cycles.*
2. *Maximum value measured at worst case conditions for both temperature and VCC.*
3. *Block size is different: 128 KWord for M29DW128G, 32 KWord for M29DW128F.*
4. *Enhanced Buffered Program with VPP/WP = VPP for M29DW128G and Quadruple Word for M29DW128F.*

5 Block protection

In M29DW128F, there are three techniques that can be used to control block protection, these are the programmer technique, the in-system technique and temporary no protection. In M29DW128G, there are three more sophisticated software protections, such as volatile protection, non-volatile protection, and password protection (please refer to the M29DW128G datasheet for details).

The M29DW128F and M29DW128G both feature hardware protection. In particular, the V_{PP}/\overline{WP} pin protects the highest block of the M29DW128FH and M29DW128GH (01 model), and the lowest block of the M29DW128FL and M29DW128GL (02 model).

5.1 Temporary block unprotect

In the M29DW128F, when held at V_{ID} , the Reset/Block Temporary Unprotect pin, \overline{RP} , will temporarily unprotect all the blocks previously protected using a high voltage block protection technique. In the M29DW128G, this functionality is available upon customer request.

6 Extended memory block

The M29DW128F has a 128Words/256Bytes extended memory block, with 64 Words / 128 Bytes Factory Locked and 64 Words / 128 Bytes Customer Lockable. The M29DW128G has a bigger Extended Memory block with 256 Words, divided in 128 Words Factory Locked and 128 Words Customer Lockable.

7 Conclusion

M29DW128G pinout is compatible with M29DW128F. Both products use the same basic command interface.

Users that are migrating the design from M29DW128F to M29DW128G must take in consideration the main differences between the two devices: blocks architecture, device ID, V_{PPH} supply voltage and x8 memory organization in TSOP package.

Applications can be easily migrated from an M29DW128F to an M29DW128G Flash memory. Despite not being a full replacement of the M29DW128F, the M29DW128G features better performance in terms of programming / erasing time and protections

8 Revision history

Table 11 Document revision history

| Date | Version | Changes |
|-----------------|---------|------------------|
| 26-January-2007 | 1 | Initial release. |

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