



Conversion Guide: Numonyx™ StrataFlash® Wireless Memory (L18) 130 nm to 65 nm

Application Note - 903

May 2008

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH NUMONYX™ PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN NUMONYX'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, NUMONYX ASSUMES NO LIABILITY WHATSOEVER, AND NUMONYX DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF NUMONYX PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. Numonyx products are not intended for use in medical, life saving, life sustaining, critical control or safety systems, or in nuclear facility applications.

Numonyx B.V. may make changes to specifications and product descriptions at any time, without notice.

Numonyx B.V. may have patents or pending patent applications, trademarks, copyrights, or other intellectual property rights that relate to the presented subject matter. The furnishing of documents and other materials and information does not provide any license, express or implied, by estoppel or otherwise, to any such patents, trademarks, copyrights, or other intellectual property rights.

Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Numonyx reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

Contact your local Numonyx sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an order number and are referenced in this document, or other Numonyx literature may be obtained by visiting the Numonyx website at <http://www.numonyx.com>.

Numonyx, the Numonyx logo, and StrataFlash are trademarks or registered trademarks of Numonyx B.V. or its subsidiaries in other countries.

*Other names and brands may be claimed as the property of others.

Copyright © 2008, Numonyx, B.V., All Rights Reserved.

Contents

1.0	Introduction	5
2.0	Device Overview	5
2.1	L18 130nm Device Overview	5
2.2	L18 65nm Device Overview	5
2.3	L18-130nm vs. L18-65nm Features Comparison	6
3.0	Device Packaging and Ballout	6
3.1	QUAD+ Ballout	7
3.2	x16D Ballout	8
4.0	Hardware Design Considerations	9
4.1	AC Read Specifications	9
4.2	AC Write/Erase Specifications	9
4.3	DC Current Specification	10
5.0	Flash Software Design Considerations	11
5.1	Memory Partitioning	11
5.2	Device Identification	11
5.3	Read Configuration Register (RCR)	12
5.4	Enhanced Configuration Register	13
5.5	Blank Check	13
5.6	Device Commands	14
5.7	WAIT State Comparison	14
5.8	CFI Differences	16
6.0	Conversion Considerations	18
6.1	Flash Data Integrator (FDI)	18
A	Additional Information	18

Revision History

Date of Revision	Revision	Description
February 2007	01	Initial Release
May 2008	02	Applied Numonyx branding.

1.0 Introduction

This application note describes converting from the Numonyx™ StrataFlash® Wireless Memory (L18-130nm) to the Numonyx StrataFlash® Wireless Memory (L18-65nm).

Note:

Unless otherwise indicated, throughout the rest of this document, the Numonyx StrataFlash® Wireless Memory (L18-130nm) device is referred to as the L18-130nm. The Numonyx StrataFlash® Wireless Memory (L18-65nm) device is referred to as the L18-65nm.

This document was written based on device information available at the time. Any changes in specifications to either device might not be reflected in this document. Refer to the appropriate documents or sales personnel for the current product information before finalizing any design.

2.0 Device Overview

The following sections provide a brief overview of the feature differences between Numonyx L18-130nm & L18-65nm devices.

2.1 L18 130nm Device Overview

The Numonyx StrataFlash® Wireless Memory (L18-130nm) device is available in 128-, and 256-Mbit densities. Its advanced features include multiple I/O voltage ranges, new array blocks and partition architectures, Buffered Enhanced Factory Programming, expanded OTP register space, and AC/DC specifications for 54 MHz operation with initial access of 85 ns.

L18-130nm is also available in the QUAD+ SCSP package with additional flash and RAM stacked within the same package.

2.2 L18 65nm Device Overview

The Numonyx StrataFlash® Wireless Memory (L18-65nm) device is available in 256-, and 512-Mbit densities. The feature set for L18-65nm is similar to L18-130nm. The key differences being L18-65nm supports only the 1.8V voltage range. It has both symmetrical (512-Mbit) and asymmetrical (256-Mbit) block architecture. The AC/DC specifications supports up to 110 MHz operation, and the initial access time has increased to 100 ns.

L18-65nm is also available in multiple SCSP packages with additional flash and RAM stacked within the same package.

2.3 L18-130nm vs. L18-65nm Features Comparison

Table 1: Feature Comparison

Features / Specifications		L18-130nm	L18-65nm
Available Densities (Monolithic)	128Mbit	Yes	No
	256Mbit	Yes	Yes
	512Mbit	No	Yes
Block Architecture	Parameter Blocks	Four: 32-kByte (128-, 256-Mb)	Four: 32-kByte (256Mb) No Param Blocks (512Mb)
	Main Blocks	128-kByte	128-kByte
	16-bit data bus	Yes	Yes
Operating Voltage	Logic Core (V _{CC})	1.7 V to 2.0 V	1.7 V to 2.0 V
	I/O (V _{CCQ})	1.7 V to 2.0 V	1.7 V to 2.0 V
Features	Read-While-Write/Erase	Yes	Yes
	OTP Register Space	128 bits + 2 Kbits	128-bits + 2 Kbits
	Flexible Block Locking	Yes	Yes
	Blank Check	No	Yes
Reliability	Operating Temperature	-25 °C to +85 °C	-25 °C to +85 °C
	Cycles	100,000	100,000
Interface	Non-Mux	Yes	Yes
	A/D-Mux	Yes	Yes

3.0 Device Packaging and Ballout

The following section provide a brief overview of the package and ballout differences between Numonyx™ StrataFlash® Wireless Memory (L18-130nm) and Numonyx StrataFlash® Wireless Memory (L18-65nm) devices.

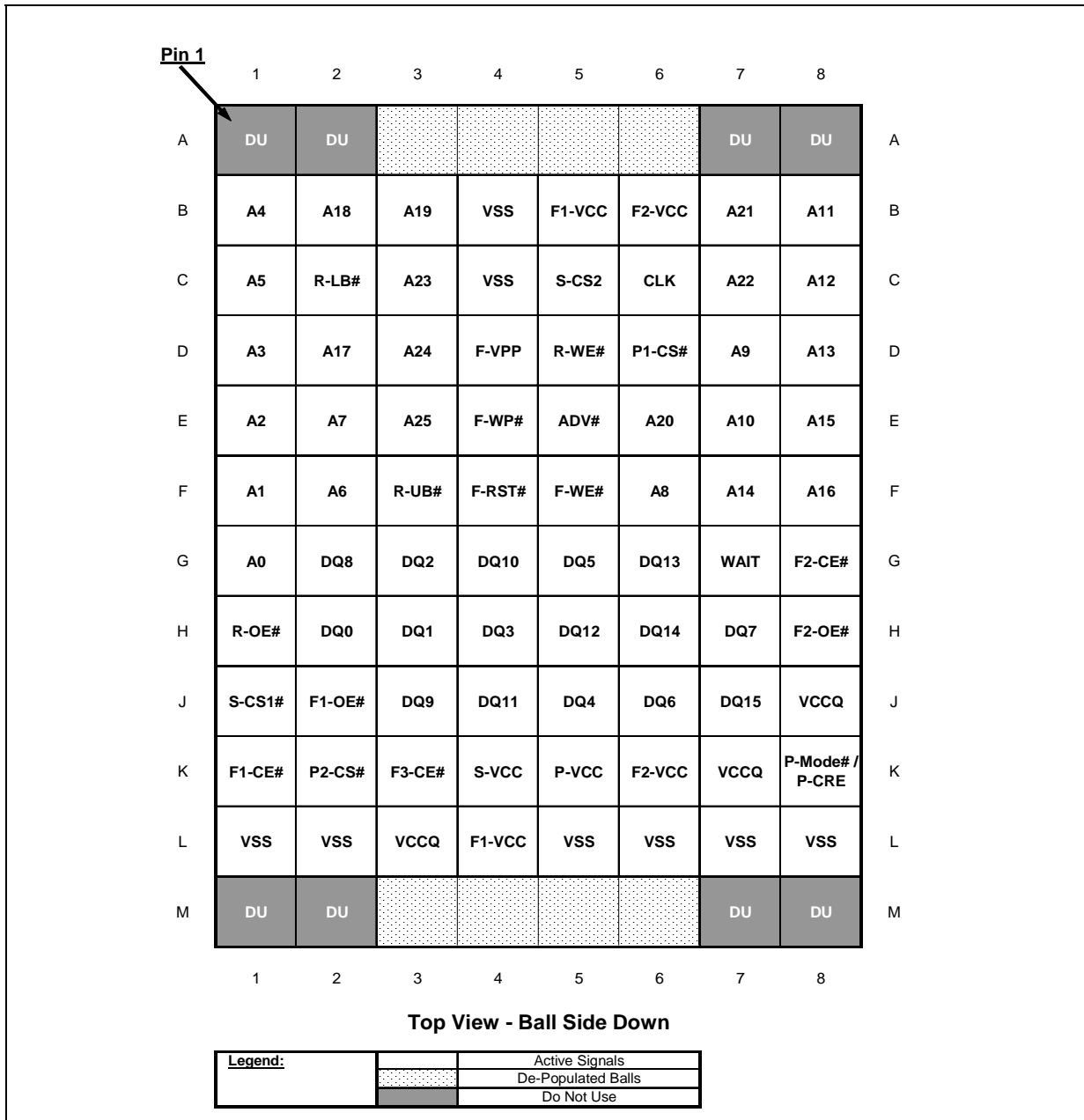
Table 2: Package Comparison

Features / Specifications		L18-130nm	L18-65nm
Packaging	VF BGA (discrete only)	Yes	No
	QUAD+ (SCSP)	Yes	Yes
	x16D (SCSP)	Yes	Yes

3.1 QUAD+ Ballout

The QUAD+ ballout is available on L18-130nm & L18-65nm SCSP products. Control signals for L18-130nm, L18-65nm, SRAM, and PSRAM are defined for the QUAD+ ballout (see Figure 1). The solder-ball pitch of the QUAD+ ballout is 0.8 mm, and uses an 8 x 10 active-ball matrix. Additional solder balls (DUs) are positioned at each corner of the package for board-level reliability.

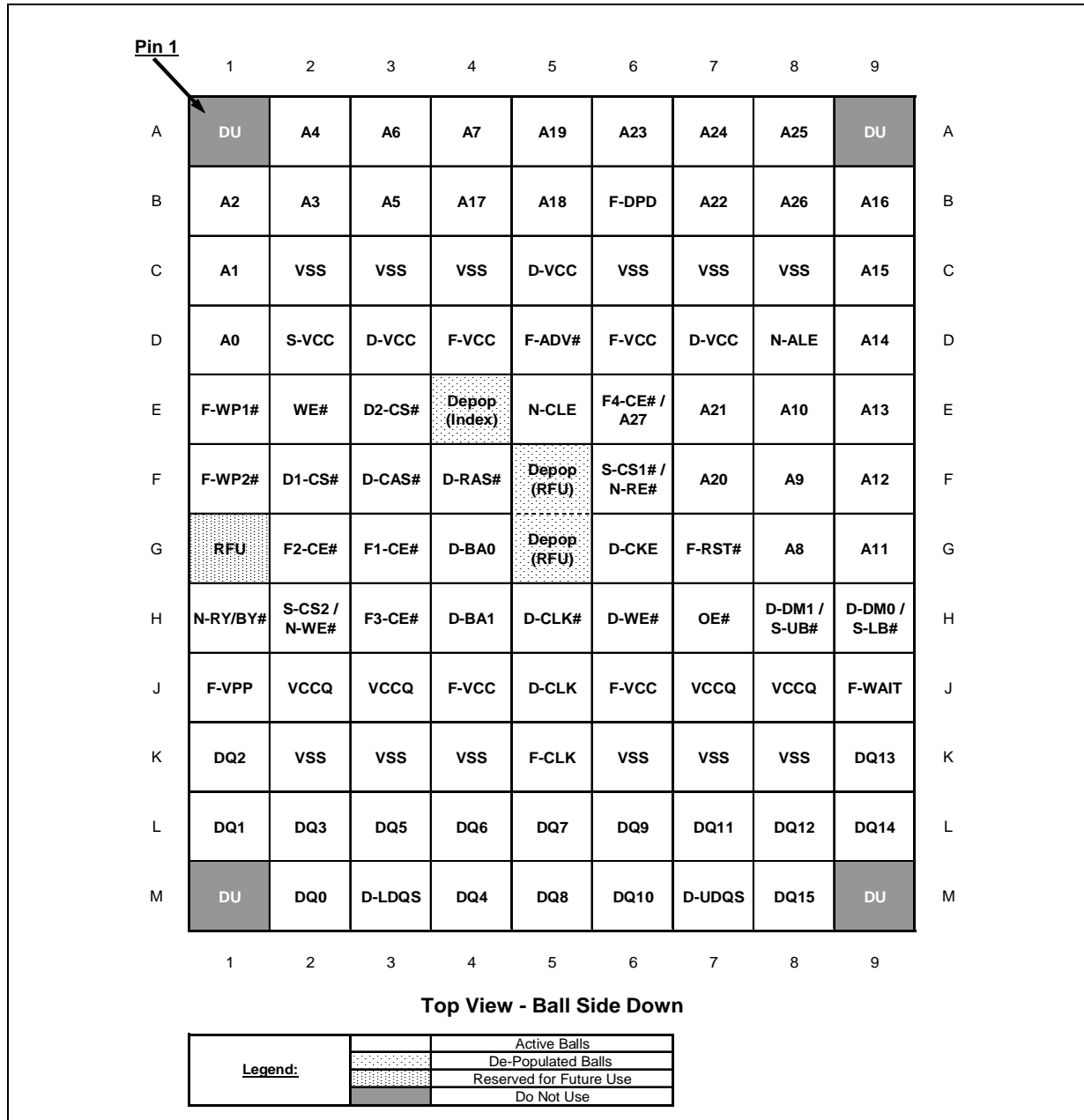
Figure 1: QUAD+ Ballout and Signals



3.2 x16D Ballout

The x16D ballout supports L18-65nm SCSP products. Control signals for L18-65nm and SDRAM are defined in the x16D ballout (see Figure 2). The solder-ball pitch of the x16D ballout is 0.8 mm, and it uses a 105 active-ball matrix. Additional solder balls (DUs) are positioned near each corner of the package for board-level reliability.

Figure 2: x16D Ballout and Signals



4.0 Hardware Design Considerations

The L18-130nm and L18-65nm flash memory devices provide low voltage, high performance operation for wireless applications, satisfying the need for increasing data-transfer speeds, reduction in overall system power consumption, and cost. Both flash devices feature multi-partition architecture, hardware read-while-write functionality, and 1.8 V operation. Although the L18-130nm and L18-65nm flash devices have same hardware interfaces. The following sections discuss hardware design considerations when converting from the L18-130nm device to the L18-65nm device.

4.1 AC Read Specifications

Note: Refer to the product datasheet for detailed list of all read timing specifications.

- Numonyx™ StrataFlash® Wireless Memory (L18): (order number 251902)
- Numonyx StrataFlash® Wireless Memory (65nm L18): (order number 318604)

Table 3: Key AC Read Spec Comparison

Features / Specifications		L18-130nm	L18-65nm
Performance	Clock Frequency (Max)	54MHz	110 MHz
	Asynchronous Access (t_{AVQV} t_{VLQV} t_{ELQV})	85 ns	100 ns
	Asynch Page Access time (t_{APA})	25 ns	15 ns
	Clock-to-Data Burst Access (t_{CHQV})	14 ns	9 ns (\leq 83 MHz) 6ns (>83 Mhz)
	Burst Data Hold Time (t_{CHOX})	3 ns	3 ns (\leq 83 MHz) 2ns (>83 Mhz)
	Address & ADV# Setup Time (t_{AVCH} , t_{VLCH})	7 ns	3 ns
	CE# Setup Time (t_{ELCH})	7 ns	4 ns
	Rise/Fall Time ($t_{FCLK/LCLK}$)	3.0 ns	3.0 ns \leq 66 MHz 2.5 ns > 66 MHz
	Clock High/Low Time ($t_{CH/CL}$)	4.05 ns	3.03 ns
	Program Suspend (typ/max)	20 ns / 25 ns	20 ns / 25 ns
	Erase Suspend (typ/max)	20 ns / 25 ns	20 ns / 25 ns
	Async Page Size	4 words	16 words
	Synchronous Burst Length (word)	4-, 8-, 16-, and Cont.	4-, 8-, 16- and Cont.
	Burst Suspend Mode	Yes	Yes

4.2 AC Write/Erase Specifications

Note: Refer to the product datasheet for detailed list of all write and erase timing specifications.

- Numonyx StrataFlash® Wireless Memory (L18): (order number 251902)
- Numonyx StrataFlash® Wireless Memory (65nm L18): (order number 318604)

Table 4: Key AC Read Spec Comparison

Features / Specifications		L18-130nm	L18-65nm
Program Performance	Program Buffer Size	64 Bytes	1024 Bytes
	Single Word Program Time (typ/max)	90/180 µs	135/350 µs
	Buffered Program Time (typ/max)	440/880 µs (64 Bytes)	160/700 µs (64 Bytes) 380/1675 µs (512 Bytes) 685/3000 µs (1024 Bytes)
Erase Performance	Erase Time - 16KW Param. Block (typ/max)	0.4/2.5 s	0.8/4.0 s
	Program/Erase Suspend Latency (typ/max)	20/25 µs	20/25 µs
	Blank Check	No	Yes

4.3 DC Current Specification

The L18-65nm device consumes higher power than the L18-130nm device during read cycles and in standby mode. This current is higher due to the read bandwidth being 16-words for L18-65nm vs. 4-words for L18-130nm. The larger bandwidth provides L18-65nm with faster burst frequency and longer word-line regulation.

Table 5: Key AC Read Spec Comparison

Features / Specifications		L18-130nm	L18-65nm
DC Current Characteristics	Standby Current (typ/max)	20/70 µA (128Mb) 25/110 µA (256Mb)	50/130 µA (256Mb) 55/160 µA (512Mb)
	Continuous Burst Read Current (typ/max)	22/27 mA (54MHz)	21/24 mA (66MHz) 30/39 mA (110MHz)
	Program/Erase Current (typ/max)	35/50 mA	35/50 mA

5.0 Flash Software Design Considerations

The following sections discuss software design considerations when converting from the L18-130nm device to the L18-65nm device.

5.1 Memory Partitioning

The L18-130nm flash array has asymmetrical physical partitioning and blocking architecture.

- 128-Mbit device (130nm) contains 16 partitions with partition size of 8Mbit. One parameter partition (top/bottom) contains four 32-kByte parameter blocks and seven 128-kByte main blocks. The remaining main partition contain eight 128-kByte main blocks each.
- 256-Mbit device (130nm) contains 16 partitions with partition size of 16Mbit. One parameter partition (top/bottom) contains four 32-kByte parameter blocks and fifteen 128-kByte main blocks. The remaining main partition contain sixteen 128-kByte main blocks each.

The L18-65nm flash array has symmetrical & asymmetrical physical partitioning and blocking architecture. The 256-Mbit device has asymmetrical partitioning, while the 512-Mbit symmetrical blocking architecture with its main array organized into equal-size.

- 256-Mbit device (65nm) contains 16 partitions with partition size of 16Mbit. One parameter partition (top/bottom) contains four 32-kByte parameter blocks and fifteen 128-kByte main blocks. The remaining main partition contain sixteen 128-kByte main blocks each.
- 512-Mbit device (65nm) contains 16 partitions with partition size of 32Mbit. Every partition contains the same block size set at 128-kByte.

5.2 Device Identification

The L18-130nm and L18-65nm flash devices each has its own unique device identification code. System software can be pre-enabled for L18-65nm by inserting conditional jumps to device-specific routines based on the device ID code that is read during system initialization. [Table 6, "L18 Device ID Codes"](#) show the device IDs for available L18-130nm and L18-65nm devices.

Table 6: L18 Device ID Codes

Code Type	Address Offset	Device Density	L18-130nm Codes		L18-65nm Codes	
			Top	Bottom	Top	Bottom
Non-Mux Device Identification	0x01	128 Mbit	880C	880F	N/A	N/A
		256 Mbit	880D	8810	8987	8989
		512 Mbit	N/A	N/A	898A	
A/D-Mux Device Identification	0x01	128 Mbit	8809	8835	N/A	N/A
		256 Mbit	880A	8836	8981	8985
		512 Mbit	N/A	N/A	8982	

5.3 Read Configuration Register (RCR)

Similar to the L18-130nm device, configuring the L18-65nm device's Read Configuration Register (RCR) puts the device in synchronous burst-read mode. However, the L18-65nm RCR has changed from that used on L18-130nm. Changes for L18-65nm include:

- Latency Count *RCR[14:11]*: an additional bit, RCR14, has been added; RCR14 was reserved on L18-130nm. L18-65nm supports latency counts of 8, 9, 10, 11, 12, 13, 14, and 15.
- Wait Polarity *RCR[10]*: L18-130nm default setting high and L18-65nm default setting is low.
- Data Hold *RCR[9]*: L18-130nm support 1-clock or 2-clock cycle data hold. L18-65nm is reserved and only supports data hold of one cycle only.
- Wait Delay *RCR[8]*: Same values for L18-130nm & L18-65nm.
- Burst Sequence *RCR[7]*: L18-130nm supports Linear "1" and Numonyx "0" burst order. L18-65nm supports linear "0" only. Setting L18-65nm to "1" will not affect the burst order; the burst order will always be linear.
- Clock Edge *RCR[6]*: Same values for L18-130nm & L18-65nm.
- Reserved *RCR[5:4]*: Same values for L18-130nm & L18-65nm.
- Burst Wrap *RCR[3]*: Same values for L18-130nm & L18-65nm.
- Burst Length *RCR[2:0]*: Same values for L18-130nm & L18-65nm.

Note: The differences are summarized in the table below.

Table 7: Read Configuration Register Differences

Register Field	Value	L18-130nm	L18-65nm
Latency Count	1000 = Code 8 1001 = Code 9 1010 = Code 10 1011 = Code 11 1100 = Code 12	NA	Available
Wait Polarity	0 =WAIT signal is active low 1 =WAIT signal is active high	Default High	Default Low
Data Hold	0 =Data held for a 1-clock data cycle 1 =Data held for a 2-clock data cycle	Available	1-clock cycle only
Burst Sequence	0 =Reserved 1 =Linear	Numonyx Burst Order Linear Burst Order	Linear Burst Order
Clock Edge	0 = Falling edge 1 = Rising edge	Available	Available
Burst Wrap	0 =Wrap; Burst accesses wrap within burst length set by BL[2:0] 1 =No Wrap; Burst accesses do not wrap within burst length	Available	Available
Burst Length	001 =4-word burst 010 =8-word burst 011 =16-word burst 111 =Continuous-word burst	Available	Available

5.4 Enhanced Configuration Register

The Enhanced Configuration Register (ECR) is a new register for the L18-65nm device. The ECR is a volatile 16-bit, read/write register used to modify the clock to output delay setting and the output-driver strength of the flash device. Upon power-up or exit from reset, the Enhanced Configuration Register defaults to 0004h.

Note: Refer to the L18-65nm datasheet for a full explanation of settings and configurations.

Table 8: Clock to output delay setting

ECR[4:3]	TCHQV/TCHQV	TCHQX/TCHTX	Frequency
0 0 = Code 0 (default)	9.0ns	3.0 ns	LC _≤ 8, <83 MHz
	6.0ns	2.0 ns	LC _≥ 9, 83.3 MHz
0 1 = Code 1	Reserved		
1 0 = Code 2	9.0ns	3.0 ns	LC _≤ 8, <83 MHz
1 1 = Code 3	6.0ns	2.0 ns	LC _≥ 9, 83.3 MHz

Table 9: Output driver control characteristics

Control Bits ECR[2:0]	Impedance @ VCCQ/2 (Ohm)	Driver Multiplier	Load Driven at Same Speed (pF)
001	90	1/3	10
010	60	1/2	15
011	45	2/3	20
100 (default)	30	1	30
101	20	3/2	35
110	15	2	40

5.5 Blank Check

Blank Check is used to see if a main-array block is completely erased. A Blank Check operation is performed one block at a time, and cannot be used during Program Suspend or Erase Suspend.

To use Blank Check, first issue the Blank Check setup command followed by the confirm command. The read mode of the addressed partition is automatically changed to Read Status Register mode, which remains in effect until another read-mode command is issued. During a blank check operation, the Status Register indicates a busy status (SR7 = 0). Upon completion, the Status Register indicates a ready status (SR7 = 1).

Note: Issuing the Read Status Register command to another partition switches that partition's read mode to Read Status Register mode, thereby allowing the blank check operation to be monitored from that partition's address.

The Status Register should be checked for any errors, and then cleared. If the Blank Check operation fails, i.e., the block is not completely erased, then the Status Register will indicate a Blank Check error (SR[7,5] = 1).

5.6 Device Commands

L18-65nm is fully compatible from a command set perspective. The only considerations than need to be taken are for new features and registers; blank check operation and Enhanced configuration operation. Table 11 shows a comparison of the L18-130nm & L18-65nm.

Table 10: Command Bus Operations

Command		L18-130nm Code (Setup/Confirm)	L18-65nm Code (Setup/Confirm)
Read Modes	Read Array	00FFh	00FFh
	Read Status Register	0070h	0070h
	Clear Status Register	0050h	0050h
	Read Device Information	0090h	0090h
	CFI Query	0098h	0098h
Program/Erase Operations	Word Program	0040h	0040h
	Buffered Program	00E8h/00D0h	00E8h/00D0h
	Buffered Enhanced Factory Program	0080h/00D0h	0080h/00D0h
	Block Erase	0020h/00D0h	0020h/00D0h
	Program/Erase Suspend	00B0h	00B0h
	Program/Erase Resume	00D0h	00D0h
	Blank Check	N/A	00BCh/00D0h
Security	Lock Block	0060h/0001h	0060h/0001h
	Unlock Block	0060h/00D0h	0060h/00D0h
	Lock Down Block	0060h/002Fh	0060h/002Fh
Registers	Program Read Configuration Register	0060h/0003h	0060h/0003h
	Program Enhanced Configuration Register	N/A	0060h/0004h
	Program OTP Register	00C0h	00C0h

5.7 WAIT State Comparison

This section will compare the difference between the WAIT states on the L18-130nm and the L18-65nm.

5.7.1 WAIT State L18-130nm

After encountering an end-of-wordline situation, periodic wait states can occur in general as illustrated in [Figure 3, "Periodic Wait State Timing Diagram" on page 15](#). [Table 11, "Periodic Data and Wait State Comparison" on page 15](#) shows that L18-130nm has periodic WAIT states, but L18-65nm does not.

Figure 3: Periodic Wait State Timing Diagram

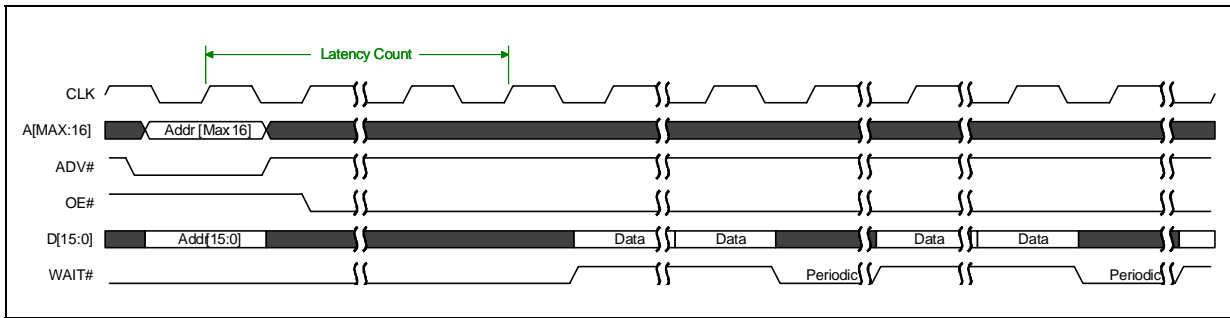


Table 11: Periodic Data and Wait State Comparison

Latency Count	L18-130nm		L18-65nm	
	Data States	Wait States	Data States	Wait States
1	Not Supported	Not Supported	Not Supported	Not Supported
2	4	0	Not Supported	Not Supported
3	4	0	16	0
4	4	0	16	0
5	4	1	16	0
6	4	2	16	0
7	4	3	16	0
8	Not Supported	Not Supported	16	0
9			16	0
10			16	0
11			16	0
12			16	0
13			16	0
14			16	0
15			16	0

5.7.2 WAIT State L18-65nm

End of wordline (EOWL) WAIT states can result when the starting address of the burst operation is not aligned to a 16-word boundary (i.e. A[3:0] of start address does not equal 0x0). Figure 4, "End of Wordline Timing Diagram" on page 16 illustrates the end of wordline WAIT state(s), which occur after the first 16-word boundary is reached. The number of data words and the number of WAIT states is summarized in Table 12, "End of Wordline Data and Wait State Comparison" on page 16 for both L18-130nm and L18-65nm.

Figure 4: End of Wordline Timing Diagram

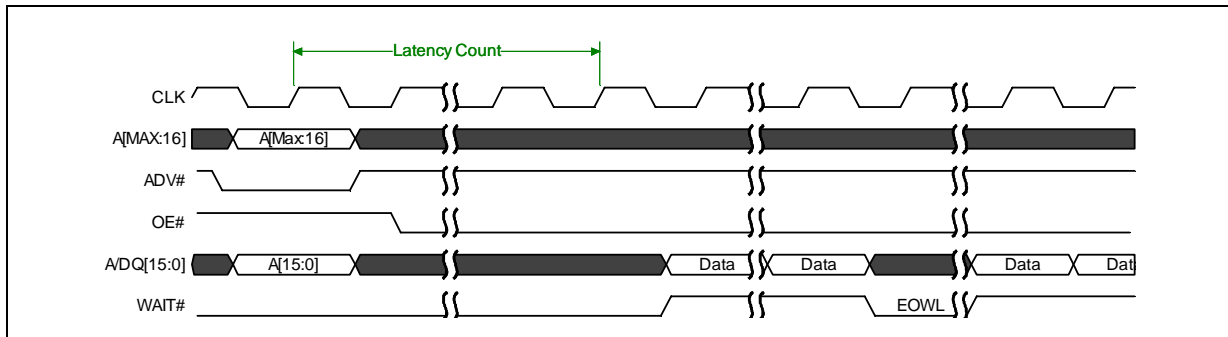


Table 12: End of Wordline Data and Wait State Comparison

Latency Count	L18-130nm		L18-65nm	
	Data States	Wait States	Data States	Wait States
1	Not Supported	Not Supported	Not Supported	Not Supported
2	4	0 to 1	Not Supported	Not Supported
3	4	0 to 2	16	0 to 2
4	4	0 to 3	16	0 to 3
5	4	0 to 4	16	0 to 4
6	4	0 to 5	16	0 to 5
7	4	0 to 6	16	0 to 6
8	Not Supported	Not Supported	16	0 to 7
9			16	0 to 8
10			16	0 to 9
11			16	0 to 10
12			16	0 to 11
13			16	0 to 12
14			16	0 to 13
15			16	0 to 14

5.8 CFI Differences

L18-65 has a different CFI revision. During adoption of own/third party software several differences need to be taking into account. This section will describe the changes.

5.8.1 CFI revision

The CFI minor revision sorted in offset (P+4)h was changed from 3 to 5.

CFI version 1.5 is supported in the software provided by Numonyx.

5.8.2 Partition Region Tables 1 and 2

If your software uses information from Partition Region Tables 1 or 2 of the CFI table please take into account following changes:

Partition Region Table1:

- New fields added into P+24h - P+25h (Bottom), P+34h - P+39h (Bottom), P+43h - P+47h (Bottom) offsets
- Fields from CFI 1.3 P+24h – P+31h (Bottom) moved down to P+26h – P+33h (Bottom) in CFI 1.5
- Fields from CFI 1.3 P+32h – P+39h (Bottom) moved down to P+3Ah – P+41h (Bottom) in CFI 1.5

Partition Region Table2:

- New fields added into offsets;
- P+48h - P+49h (Bottom), P+3A - P+3Bh (Top)
- P+58h - P+5Dh (Bottom), P+4A - P+4Fh (Top)
- P+58h - P+5Dh (Top)
- Fields from CFI 1.3 P+3Ah – P+47h (Bottom), P+32h – P+3Fh (Top), moved down to P+4Ah – P+57h (Bottom), P+3Ch – P+49h (Top) in CFI 1.5
- Fields from CFI 1.3 P+40h – P+47h (Top) moved down to P+50h – P+57h (Top) in CFI 1.5

5.8.3 Performance improvements in L18-65

Write performance can be increased by using write buffer up to 1024 bytes (2Ah).

Read performance can be improved by providing read page buffer up to 32 bytes (P+1Dh).

5.8.4 Time-out changes in CFI 1.5

All changes are listed in [Table 13, "Value Changes in CFI 1.5"](#)

Table 13: Value Changes in CFI 1.5

Num	Difference	CFI 1.3		CFI 1.5	
		offset	value	offset	value
1	"n" such that typical single word program time-out = 2n μ-sec	1Fh	08	1Fh	07
2	"n" such that typical max. buffer write time-out = 2n μ-sec	20h	09	20h	0A
3	"n" such that maximum word program time-out = 2n times typical	23h	01	23h	08
4	"n" such that maximum buffer write time-out = 2n times typical	24h	01	24h	0B
5	"n" such that maximum number of bytes in write buffer = 2 ⁿ	2Ah	64	2Ah	1024

6.0 Conversion Considerations

The Numonyx low level driver today does not support the following features:

- Write while Erase

The low level drivers default to page mode. L18-65nm has a bigger program buffer size which greatly improves the write performance. Users should use appropriate program and read modes to accomplish this.

6.1 Flash Data Integrator (FDI)

Support of L18-65 is planned in FDI 7.3.5 and later releases.

Appendix A Additional Information

Order/Document Number	Document/Tool
251902	Numonyx™ StrataFlash® Wireless Memory (L18) Datasheet
318604	Numonyx™ StrataFlash® Wireless Memory (65nm L18) Datasheet

Note: Contact your local Numonyx or distribution sales office or visit the Numonyx World Wide Web home page at <http://www.Numonyx.com> for technical documentation, tools, and additional information.