



Technical Note

Comparing Micron N25Q and Winbond W25Q Flash Devices

Introduction

The purpose of this technical note is to compare features of the Micron[®] N25Q (32Mb or 64Mb) and Winbond W25Q Flash memory devices. Features compared include memory architecture, package options, signal descriptions, command sets, electrical specifications, and device identification.



Memory Array Architecture

N25Q Features	W25Q Features
Program 1 to 256 bytes	Program 1 to 256 bytes
Uniform sector erase (64KB)	Uniform sector erase (32KB and 64KB)
Uniform subsector erase (4KB)	Uniform subsector erase (4KB)

Package Configurations

Table 1: Package Configurations

Package	N25Q		W25Q	
	32Mb	64Mb	32Mb	64Mb
VDFPN8 (8mm x 6mm MLP8)	Yes	Yes	Yes	Yes
TBGA24 (6mm x 8mm)	Yes	Yes	–	–
VDFPN8 (6mm x 5mm MLP)	Yes	Yes	Yes	Yes
SO16 (300 mils body width)	Yes	Yes	Yes	Yes
SO8W (SO8 208 mils body width)	Yes	Yes	Yes	Yes
UDFPN8 (4mm x 3mm MLP)	Yes	–	–	–
SO8N (SO8 150 mils body width)	Yes	–	Yes	–

Signal Descriptions

Table 2: Signal Descriptions

N25Q Signal	W25Q Signal	Type	Description
C	CLK	Input	Serial clock
DQ0	DI (IO0)	Input or I/O	Serial data input or I/O
DQ1	DO (IO1)	Output or I/O	Serial data output or I/O
S#	#CS	Input	Chip select
W/V _{pp} /DQ2	#WP (IO2)	Input or I/O	Write protect/enhanced program supply voltage or I/O
HOLD#/DQ3	#HOLD (IO3)	Input or I/O	HOLD or I/O
V _{CC}	V _{CC}	Input	Supply voltage
V _{SS}	GND	Input	Ground

- Notes:
1. During quad I/O operation, the W25Q must set a bit (QE in SR2) for quad I/O functionality; during that time, #WP and #HOLD are disabled.
 2. During quad I/O operation, N25Q must set a bit (VCR or NVCR) for quad I/O functionality; during that time, the W and HOLD signals are functional. The W and HOLD signals lose functionality only when quad I/O operations are in progress (QUAD OUTPUT FAST READ, QUAD I/O FAST READ, and QUAD INPUT FAST PROGRAM).

Commands

Table 3: Supported Command Set

Command Name	Command Code (Setup/Confirm) N25Q	Command Code (Setup/Confirm) W25Q	Notes
READ			
READ	03h	03h	
FAST READ	0Bh	0Bh	
DUAL OUTPUT FAST READ	3Bh	3Bh	
DUAL INPUT/OUTPUT FAST READ	BB	BB	
QUAD OUTPUT FAST READ	6Bh	6Bh	
QUAD INPUT/OUTPUT FAST READ	EBh	EBh	
READ DEVICE ID	9Fh/9Eh	9Fh	1
READ ELECTRONIC SIGNATURE	N/A	ABh/90h	2
OCTAL WORD READ QUAD I/O	N/A	E3h	2
CONTINUOUS READ MODE	N/A	FFh	2
PROGRAM			
PAGE PROGRAM	02h	02h	
DUAL INPUT FAST PROGRAM	A2h	N/A	3
QUAD INPUT FAST PROGRAM	32h	32h	
ERASE			
BULK ERASE	C7h	C7h/60h	4
SECTOR ERASE – 64KB	D8h	D8h	
SECTOR ERASE – 32KB	N/A	52h	2
SUBSECTOR ERASE – 4KB	20h	20h	
SUSPEND			
PROGRAM/ERASE SUSPEND	75h	75h	
PROGRAM/ERASE RESUME	7Ah	7Ah	
DEEP POWER-DOWN			
DEEP POWER-DOWN	B9h	B9h	5, 6
RELEASE FROM DEEP POWER-DOWN	ABh	ABh	5, 6

- Notes:
1. 9Eh not supported on the W25Q.
 2. Not supported on the N25Q.
 3. Not supported on the W25Q.
 4. 60h not supported on the N25Q.
 5. Commands are used to place the device in low power consumption mode.
 6. Only available on the 1.8V N25Q, not on the 3V N25Q.

READ Commands

The READ command set for the N25Q and W25Q devices is identical, and each device follows the standard three address byte protocol.

The W25Q has a fixed dummy cycle read, but the N25Q dummy cycles can be configured and controlled in the nonvolatile configuration register (NVCR), bits 12 to 15, or in the volatile configuration register (VCR), bits 7 to 4.

W25Q requires a nonvolatile QE bit in the SR2 to enable the quad I/O functionality, and when this bit is set, the W and HOLD pins are disabled. VECR or NVCR enables the QSPI protocol (refer to the data sheet for more details). QUAD commands are available without any register setting. When VECR or NVCR bits are set, W and HOLD are still functional. With NVCR set (bit 3 = 0), the device can be powered up or down with quad I/O functionality.

The W25Q and N25Q manufacturer ID, memory type, and memory capacity can be read out by issuing a 9Fh command. N25Q will output the same data when the 9Eh command is issued; the W25Q does not support the 9Eh command.

The W25Q has commands that output the memory capacity (ABh), memory type and capacity (90h), and additional read commands, including OCTAL WORD READ QUAD I/O (E3h) and CONTINUOUS READ MODE (FFh). N25Q does not support ABh, 90h, E3h, or FFh commands.

PROGRAM Commands

The W25Q requires a nonvolatile QE bit in the SR2 to enable the quad I/O functionality; the N25Q requires the VECR or NVCR to enable the quad I/O functionality. With NVCR set (bit 3 = 0), the device can be powered up or down with quad I/O functionality. The N25Q also has dual I/O commands (A2h) that are not supported by the W25Q.

ERASE Commands

The W25Q has a 32KB SECTOR ERASE command (52h) and a FULL CHIP ERASE command (60h) that are not supported by the N25Q.

Execute in Place (XIP)

The protocol for execute in place (XIP) is different for the two devices. N25Q XIP is configured by selecting the appropriate line item or by issuing the correct confirmation command, whereas the W25Q XIP is enabled by issuing the correct confirmation command. Refer to Application Note, "Using XIP Modes in the Forte™ N25Q Flash Memory Device."

Figure 1: XIP Timing Configuration

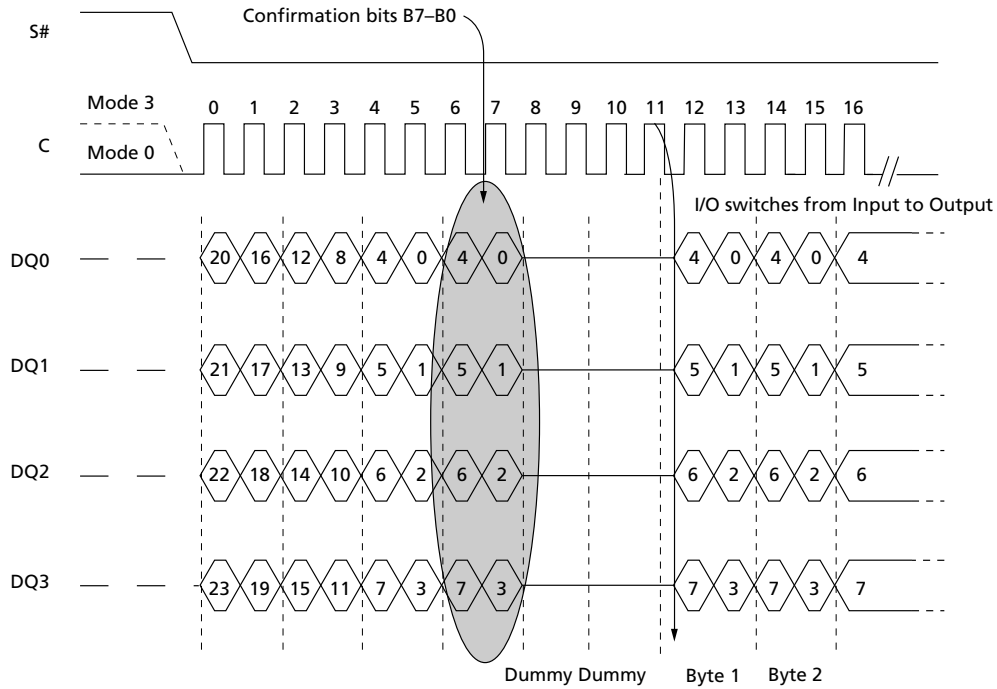


Table 4: XIP Confirmation Bit Software Commands

XIP Confirmation Bit	N25Q	W25Q
Enter/confirm XIP mode	B4 = 0 (B7 to B5 and B3 to B0 = "Don't Care")	B5 to B4 = 1,0 (B7 to B6 and B3 to B0 = "Don't Care")
Exit XIP mode	B4 = 1 (B7 to B5 and B3 to B0 = "Don't Care")	B5 to B4 ≠ 1,0 (B7 to B6 and B3 to B0 = "Don't Care")



Electrical Characteristics

Table 5: DC Current Characteristics

Parameter	Symbol	N25Q		W25Q		Units
		Min	Max	Min	Max	
Standby current	I_{CC1}	–	100	25	50	μA
Operating current (FAST READ QUAD I/O)	I_{CC3}	–	20	12	18	mA
Operating current (PAGE PROGRAM)	I_{CC4}	–	20	20	25	mA
Operating current (WRITE STATUS REGISTER)	I_{CC5}	–	20	8	12	mA
Operating current (ERASE)	I_{CC6}	–	20	20	25	mA

Table 6: DC Voltage Specifications

Parameter	Symbol	N25Q		W25Q		Units
		Min	Max	Min	Max	
Input low voltage	V_{IL}	–0.5	$0.3 V_{CC}$	–0.5	$0.3 V_{CC}$	V
Input high voltage	V_{IH}	$0.7 V_{CC}$	$V_{CC} + 0.4$	$0.7 V_{CC}$	$V_{CC} + 0.4$	V
Output low voltage	V_{OL}	–	0.4	–	0.4	V
Output high voltage	V_{OH}	$V_{CC} - 0.2$	–	$V_{CC} - 0.2$	–	V



AC Specifications

Table 7: AC Specifications

Parameter	Symbol	Alternate Symbol	N25Q		W25Q		Units
			Min	Max	Min	Max	
Clock frequency (x1 FAST READ)	f _C	f _C	–	108	–	80	MHz
Clock frequency (READ)	f _R	f _R	–	54	–	33	MHz
S active setup time	t ^{SLCH}	t ^{CSS}	4	–	5	–	ns
Data-in setup time	t ^{DVCH}	t ^{DSU}	2	–	2	–	ns
Data-in hold time	t ^{CHDX}	t ^{DH}	3	–	5	–	ns
S# deselect time after correct READ (ARRAY READ to ARRAY READ)	t ^{SHSL}	t ^{CSH}	20	–	50	–	ns
S# deselect time after incorrect READ or different instruction (ERASE/PROGRAM to READ)	t ^{SHSL}	t ^{CSH}	50	–	50	–	ns
Output disable time	t ^{SHQZ}	t ^{DIS}	–	8	–	7	ns
Clock low to output valid	t ^{CLQV}	t ^V	–	7	–	7	ns
Output hold time	t ^{CLQX}	t ^{HO}	1	–	0	–	ns
HOLD to output Low-Z	t ^{HHQX}	t ^{LZ}	–	8	–	7	ns
HOLD to output High-Z	t ^{HLQZ}	t ^{HZ}	–	8	–	12	ns

Note: 1. AC specifications compare the fastest versions available at the full voltage range (2.7–3.6V).

Program and Erase Specifications

Table 8: Program and Erase Specifications

Operation	N25Q				W25Q				Units
	32Mb		64Mb		32Mb		64Mb		
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	
PAGE PROGRAM	0.5	5	0.5	5	0.7	3	0.7	3	ms
SUBSECTOR ERASE	0.3	3	0.3	3	N/A	N/A	N/A	N/A	s
SECTOR ERASE	0.7	3	0.7	3	0.3	4	0.3	4	s
BULK ERASE	30	60	60	120	7	15	15	30	s

Configuration and Memory Map

Table 9: Sectors and Subsectors by Density

Density		Sector	Subsector	Address Range			
64		127	2047	7FFFFh	7F000h		
			:	:	:		
			2032	7F0FFFh	7F0000h		
	32		63	1023	3FFFFh	3F000h	
				:	:	:	
				1008	3F0FFFh	3F0000h	
		0		0	15	0FFFFh	0F000h
					:	:	:
					4	04FFFh	04000h
					3	03FFFh	03000h
					2	02FFFh	02000h
					1	01FFFh	01000h
					0	00FFFh	00000h

Device Identification

Manufacturer identification is assigned by JEDEC. As a result, the N25Q and W25Q devices have a different manufacturer ID and memory type codes. Command 9Fh is used to read these codes in both devices.

N25Q has a unique ID (UID) composed of 17 read-only bytes, which contain the following data:

- The first byte is set to 10h.
- The next two bytes of extended device ID specify device configuration (top, bottom, or uniform architecture and hold or reset functionality).
- The next 14 bytes contain optional customized factory data. The customized factory data bytes are factory programmed.

Refer to the N25Q data sheet for more information.

Table 10: Read Identification Summary

Parameter	N25Q Code	SST26WF Code
Manufacturer ID	20h	EFh
Memory type	BAh	40h
Memory capacity	16h (32Mb), 17h (64Mb)	16h (32Mb), 17h (64Mb)

Note: 1. For 32Mb serial Flash device only.

Conclusion

Comparing the features of the Micron N25Q and W25Q Flash memory devices enables users to migrate applications from the W25Q to the N25Q.



Revision History

Rev. A – 10/10

- Initial release

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