



Technical Note

Migrating from Spansion's S25FL256S to Micron's N25Q 256Mb Flash Device

Introduction

The purpose of this technical note is to compare features of the Micron® N25Q (256Mb) and Spansion S25FL256S Flash memory devices. Features compared include memory architecture, package options, signal descriptions, command sets, electrical specifications, and device identification.



Memory Array Architecture

N25Q Features	S25FL Features
Program 1 to 256 bytes	Program 1 to 256 bytes or 1 to 512 bytes ¹
Uniform sector erase (64KB)	Uniform sector erase (256KB or 64KB) ¹
Uniform subsector erase (4KB)	Top or bottom 32 subsectors (4KB) ¹

Note: 1. Uniform 256KB option always has 512-byte page program; hybrid 4KB top/bottom and 64KB always has 256-byte page program.

Package Configurations

Table 1: Package Configurations

Package	N25Q 256Mb	S25FL256S
V-PDFN8 (8mm x 6mm)	Yes	Yes
SOP2-16/300 mil	Yes	Yes
T-PBGA24 (6mm x 8mm)	Yes	Yes

Signal Descriptions

Table 2: Signal Descriptions

N25Q Signal	S25FL Signal	Type	Description	Notes
C	SCK	Input	Serial clock	
DQ0	SO/IO1	Input or I/O	Serial data input or I/O	
DQ1	SI/SIO0/P07	Output or I/O	Serial data output or I/O	
S#	CS#	Input	Chip select	
W/V _{pp} /DQ2	WP#/IO2	Input or I/O	Write protect/enhanced program supply voltage or I/O	1
HOLD#/DQ3	HOLD#/IO3	Input or I/O	HOLD or I/O	
V _{CC}	V _{CC}	Input	Supply voltage	
V _{SS}	V _{SS}	Input	Ground	
RESET#	RESET#	Input	Hardware Reset	2

Notes: 1. V_{pp} is not available on the Spansion S25FL256S device.
2. RESET# functionality is available on devices with a dedicated part number. For the N25Q, RESET# takes the place of HOLD#.



Commands

Table 3: Command Set

Command	Command Code N25Q	Command Code S25FL	Notes
RESET Operations			
RESET ENABLE	66h	N/A	
RESET MEMORY	99h	F0h	
MODE BITS RESET	N/A	FFh	
IDENTIFICATION Operations			
READ ID	9Eh/9Fh	9Fh	
READ MANUFACTURER AND DEVICE ID	N/A	90h	
MULTIPLE I/O READ ID	AFh	N/A	
READ ELECTRONIC SIGNATURE	N/A	ABh	
READ SERIAL FLASH DISCOVERY PARAMETER	5Ah	N/A	
READ Operations			
READ	03h	03h	
FAST READ	0Bh	0Bh	
DUAL OUTPUT FAST READ	3Bh	3Bh	
DUAL INPUT/OUTPUT FAST READ	BBh	BBh	
QUAD OUTPUT FAST READ	6Bh	6Bh	
QUAD INPUT/OUTPUT FAST READ	EBh	EBh	
FAST READ, DTR	0Dh	0Dh	
DUAL OUTPUT FAST READ, DTR	3Dh	N/A	
DUAL INPUT/OUTPUT FAST READ, DTR	BDh	N/A	
QUAD OUTPUT FAST READ, DTR	6Dh	N/A	
QUAD INPUT/OUTPUT FAST READ, DTR	EDh	EDh	
4-BYTE READ	13h	13h	
4-BYTE FAST READ	0Ch	0Ch	
4-BYTE DUAL OUTPUT FAST READ	3Ch	3Ch	
4-BYTE DUAL INPUT/OUTPUT FAST READ	BCh	BCh	
4-BYTE QUAD OUTPUT FAST READ	6Ch	6Ch	
4-BYTE QUAD INPUT/OUTPUT FAST READ	ECh	ECh	
4-BYTE FAST READ, DTR	0Dh	0Eh	1
4-BYTE DUAL INPUT/OUTPUT FAST READ, DTR	BDh	BEh	1
4-BYTE QUAD INPUT/OUTPUT FAST READ, DTR	EDh	EEh	1
WRITE Operations			
WRITE ENABLE	06h	06h	
WRITE DISABLE	04h	04h	
REGISTER Operations			
READ STATUS REGISTER	05h	05h	



Table 3: Command Set (Continued)

Command	Command Code N25Q	Command Code S25FL	Notes
READ STATUS REGISTER 2	N/A	07h	
READ CONFIGURATION REGISTER	N/A	35h	
WRITE STATUS REGISTER	01h	01h	
READ LOCK REGISTER	E8h	N/A	
WRITE LOCK REGISTER	E5h	N/A	
READ FLAG STATUS REGISTER	70h	N/A	
CLEAR FLAG STATUS REGISTER	50h	30h	2
AUTO BOOT REGISTER READ	N/A	14h	
AUTO BOOT REGISTER WRITE	N/A	15h	
READ NONVOLATILE CONFIGURATION REGISTER	B5h	N/A	
WRITE NONVOLATILE CONFIGURATION REGISTER	B1h	N/A	
READ VOLATILE CONFIGURATION REGISTER	85h	N/A	
WRITE VOLATILE CONFIGURATION REGISTER	81h	N/A	
READ ENHANCED VOLATILE CONFIGURATION REGISTER	65h	N/A	
WRITE ENHANCED VOLATILE CONFIGURATION REGISTER	61h	N/A	
BANK REGISTER ACCESS	N/A	B9h	
READ EXTENDED ADDRESS REGISTER	C8h	16h	
WRITE EXTENDED ADDRESS REGISTER	C5h	17h	3
Misc. Operations			
ASP READ	N/A	2Bh	
ASP PROGRAM	N/A	2Fh	
READ DATA LEARNING PATTERN	N/A	41h	
PROGRAM NV DATA LEARNING REGISTER	N/A	43h	
WRITE VOLATILE DATA LEARNING REGISTER	N/A	4Ah	
PPB LOCK BIT WRITE	N/A	A6h	
PPB LOCK BIT READ	N/A	A7h	
DYB READ	N/A	E0h	
DYB WRITE	N/A	E1h	
PPB READ	N/A	E2h	
PPB PROGRAM	N/A	E3h	
PPB ERASE	N/A	E4h	
PASSWORD READ	N/A	E7h	
PASSWORD PROGRAM	N/A	E8h	
PASSWORD UNLOCK	N/A	E9h	
PROGRAM Operations			
PAGE PROGRAM	02h	02h	

Table 3: Command Set (Continued)

Command	Command Code N25Q	Command Code S25FL	Notes
DUAL INPUT FAST PROGRAM	A2h	N/A	
EXTENDED DUAL INPUT FAST PROGRAM	D2h	N/A	
QUAD INPUT FAST PROGRAM	32h	32h, 38h	
EXTENDED QUAD INPUT FAST PROGRAM	12h	N/A	
4-BYTE PAGE PROGRAM	02h	12h	1
4-BYTE QUAD PAGE PROGRAMMING	32h	34h	1
ERASE Operations			
4KB SUBSECTOR ERASE	20h	20h	
SECTOR ERASE	D8h	D8h	
BULK ERASE	C7h	C7h/60h	
4-BYTE 4KB SUBSECTOR ERASE	20h	21h	1
4-BYTE SECTOR ERASE	D8h	DCh	1
PROGRAM/ERASE RESUME	7Ah/7Ah	8Ah/7Ah	
PROGRAM/ERASE SUSPEND	75h/75h	85h/75h	
ONE-TIME PROGRAMMABLE (OTP) Operations			
READ OTP ARRAY	4Bh	4Bh	
PROGRAM OTP ARRAY	42h	42h	
4-BYTE ADDRESS MODE Operations			
ENTER 4-BYTE ADDRESS MODE	B7h	N/A	
EXIT 4-BYTE ADDRESS MODE	E9h	N/A	
DEEP POWER-DOWN			
DEEP POWER-DOWN	B9h	N/A	4
RELEASE FROM DEEP POWER-DOWN	ABh	N/A	4

- Notes:
1. The N25Q device requires that 4-byte addressing be enabled by opcode or default at power-up (NVCR) before the command.
 2. Program/erase error bits are cleared by CLEAR FLAG STATUS REGISTER on the N25Q device; the S25FL does the same in status register 1.
 3. The N25Q requires WREN; the S25FL also sets addressing protocol by volatile bit BAR<7>; N25Q does the same by NVCR<0> or with the EN4BYTEADD command.
 4. DEEP POWER-DOWN operation is only available on N25Q 1.8V devices.

Table 4: Different Commands Sharing Same Command Code

Command Code	N25Q 256Mb Command	S25FL256S Command
ABh	RELEASE FROM DEEP POWER-DOWN	READ ELECTRONIC SIGNATURE
B9h	DEEP POWER-DOWN	BANK REGISTER ACCESS
E8h	READ LOCK REGISTER	PASSWORD PROGRAM
E9h	EXIT 4-BYTE ADDRESS MODE	PASSWORD UNLOCK

Table 4: Different Commands Sharing Same Command Code (Continued)

Command Code	N25Q 256Mb Command	S25FL256S Command
85h	READ VOLATILE CONFIGURATION REGISTER	PROGRAM/ERASE SUSPEND
12h	EXTENDED QUAD INPUT FAST PROGRAM	4-BYTE PAGE PROGRAM

READ Commands

The READ command set for the N25Q and S25FL devices is identical, and each device follows the standard three address byte protocol.

Both N25Q and S25FL have configurable dummy cycles, in both DTR and STR. S25FL dummy cycles can be configured by configuration register bits 7 and 8; N25Q dummy cycles can be configured by nonvolatile configuration register bits 12–15 or by volatile configuration register bits 7–4.

Table 5: STR: Minimum Number of Dummy Cycles Required per Each Frequency

Note 1 applies to entire table

Frequency MHz	FAST READ		DUAL OUTPUT FAST READ		DUAL I/O FAST READ		QUAD OUTPUT FAST READ		QUAD I/O FAST READ	
	N25Q	S25FL	N25Q	S25FL	N25Q	S25FL	N25Q	S25FL	N25Q	S25FL
≤50	0	0	0	0	1	4	0	0	3	1
≤80	0	8	0	8	3	4	3	8	6	4
≤90	1	8	2	8	4	5	3	8	8	4
≤104	3	8	4	8	6	6	6	8	9	5
≤133	–	8	–	–	–	–	–	–	–	–

Note: 1. S25FL has one additional clock for mode bits in QUAD I/O FAST READ only; N25Q always has one additional clock for mode bits.

Table 6: DTR: Minimum Number of Dummy Cycles Required per Each Frequency

Note 1 applies to entire table

Frequency MHz	FAST READ		DUAL OUTPUT FAST READ		DUAL I/O FAST READ		QUAD OUTPUT FAST READ		QUAD I/O FAST READ	
	N25Q	S25FL	N25Q	S25FL	N25Q	S25FL	N25Q	S25FL	N25Q	S25FL
≤50	2	4	3	–	5	4	4	–	9	3
≤54	3	5	5	–	7	6	7	–	10	6
≤66	–	5	–	–	–	6	–	–	–	6
≤66	–	6	–	–	–	7	–	–	–	7
≤66	–	7	–	–	–	8	–	–	–	8

Note: 1. S25FL has one additional clock for mode bits in QUAD I/O FAST READ only; N25Q always has one additional clock for mode bits.

S25FL requires a nonvolatile quad bit in the CR to enable the quad I/O functionality, and when this bit is set, the HOLD# and WP# are disabled.

VECR or NVCR enables the QSPI protocol (refer to the data sheet for more details). QUAD commands are available without any register setting. When VECR or NVCR bits are set, W and HOLD are still functional. With NVCR set (bit 3 = 0), the device can be powered up or down with quad I/O functionality. No additional commands are required for N25Q to use quad or dual I/O functionality.

The S25FL and N25Q manufacturer ID, memory type, and memory capacity can be read out by issuing a 9Fh command. N25Q will output the same data when the 9Eh command is issued.

S25FL has commands that output the device ID (ABh), and a command that outputs the manufacturer ID and device ID (90h).

Execute-in-Place (XIP)

The protocol for XIP is different for each of the devices. N25Q XIP is configured by selecting the appropriate line item or by issuing the correct confirmation command, while S25FL XIP is enabled by issuing the correct confirmation command. S25FL XIP (referred to as enhanced high performance) is available for QUAD I/O FAST READ only, or for DUAL I/O FAST READ and QUAD I/O FAST READ, depending on the line item. N25Q XiP is available on all fast read commands. Refer to Application Note, "Using XIP Modes in the N25Q Flash Memory Device."

Figure 1: XIP Timing Configuration

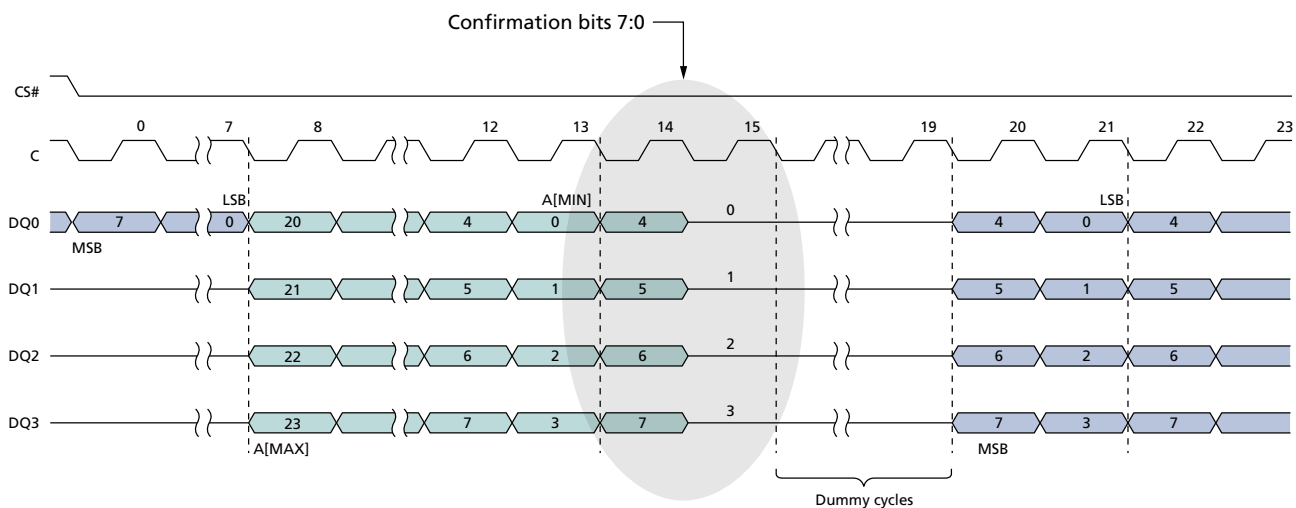


Table 7: XIP Confirmation Bit Software Commands

XIP Confirmation Bit	N25Q	S25FL
Enter/confirm XIP mode	B4 = 0 (B7–B5 and B3–B0 = "Don't Care")	Mode bits = Ah; B7 = 1; B6 = 0; B5 = 1; B4 = 0
Exit XIP mode	B4 = 1 (B7–B5 and B3–B0 = "Don't Care")	Mode bit ≠ Ah



Electrical Characteristics

Table 8: DC Current Characteristics

Parameter	Symbol	N25Q		S25FL		Units	Notes
		Min	Max	Min	Max		
Standby current	I_{CC1}	–	100	–	100	μA	1
Operating current (FAST READ QUAD I/O)	I_{CC3}	–	20	–	60	mA	
Operating current (PAGE PROGRAM)	I_{CC4}	–	20	–	100	mA	
Operating current (WRITE STATUS REGISTER)	I_{CC5}	–	20	–	100	mA	
Operating current (ERASE)	I_{CC6}	–	20	–	100	mA	

Note: 1. 300 μA if automotive grade.

Table 9: DC Voltage Specifications

Parameter	Symbol	N25Q		S25FL		Units
		Min	Max	Min	Max	
Input low voltage	V_{IL}	–0.5	$0.3 V_{CC}$	–0.5	$0.2 V_{CC}$	V
Input high voltage	V_{IH}	$0.7 V_{CC}$	$V_{CC} + 0.4$	$0.7 V_{CC}$	$V_{CC} + 0.4$	V
Output low voltage	V_{OL}	–	0.4	–	$0.15 V_{CC}$	V
Output high voltage	V_{OH}	$V_{CC} - 0.2$	–	$V_{CC} - 0.2$	–	V

AC Characteristics

Table 10: AC Specifications

Parameter	Symbol	Alternate Symbol	N25Q		S25SL		Units
			Min	Max	Min	Max	
Clock frequency (x1 FAST READ)	f _C	f _C	–	108	–	133	MHz
Clock frequency (x2, x4 FAST READ)	f _C	f _C	–	108	–	104	MHz
Clock frequency (READ)	f _R	f _R	–	54	–	50	MHz
S# active setup time	t ^{SLCH}	t ^{CSS}	4	–	8	–	ns
Data-in setup time	t ^{DVCH}	t ^{DSU}	2	–	2	–	ns
Data-in hold time	t ^{CHDX}	t ^{DH}	3	–	5	–	ns
S# deselect time after correct READ (ARRAY READ to ARRAY READ)	t ^{SHSL}	t ^{CSH}	20	–	15	–	ns
S# deselect time after incorrect READ or different instruction (ERASE/PROGRAM to READ)	t ^{SHSL}	t ^{CSH}	50	–	50	–	ns
Output disable time (2.7–3.6V)	t ^{SHQZ}	t ^{DIS}	–	8	–	8	ns
Clock low to output valid (30pF)	t ^{CLQV}	t ^V	–	7	–	8	ns
Output hold time	t ^{CLQX}	t ^{HO}	1	–	0	–	ns
HOLD to output Low-Z	t ^{HHQX}	t ^{LZ}	N/A	8	N/A	8	ns
HOLD to output High-Z	t ^{HLQZ}	t ^{HZ}	N/A	8	N/A	8	ns

Note: 1. AC specifications compare the fastest versions available at the full voltage range (2.7–3.6V).

Program and Erase Specifications

Table 11: Program and Erase Specifications

Operation	N25Q		S25FL		Unit
	Typ	Max	Typ	Max	
PAGE PROGRAM (256 bytes)	0.5	5	1.3	0.55	ms
4KB SUBSECTOR ERASE	0.3	1.5	0.13	0.65	s
64KB SECTOR ERASE	0.7	3	0.13	0.65	s
BULK ERASE	240	480	66	230	s

Configuration and Memory Map

Table 12: Sectors and Subsectors

Sector	Subsector	Address Range	
		Start	End
511	8191	01FF F000h	01FF FFFFh
	⋮	⋮	⋮
	8176	01FF 0000h	01FF 0FFFh
⋮	⋮	⋮	⋮
255	4095	00FF F000h	00FF FFFFh
	⋮	⋮	⋮
	4080	00FF 0000h	00FF 0FFFh
⋮	⋮	⋮	⋮
127	2047	007F F000h	007F FFFFh
	⋮	⋮	⋮
	2032	007F 0000h	007F 0FFFh
⋮	⋮	⋮	⋮
63	1023	003F F000h	003F FFFFh
	⋮	⋮	⋮
	1008	003F 0000h	003F 0FFFh
⋮	⋮	⋮	⋮
0	15	0000 F000h	0000 FFFFh
	⋮	⋮	⋮
	0	0000 0000h	0000 0FFFh

Device Identification

Manufacturer identification is assigned by JEDEC. As a result, the N25Q and S25FL devices have different manufacturer ID and memory type codes even though their memory capacity is identical. Command 9Fh is used to read these codes in both devices.

N25Q has a unique ID (UID) composed of 17 read-only bytes, which contain the following data:

- The first byte is set to 10h.
- The next two bytes of extended device ID specify device configuration (top, bottom, or uniform architecture and hold or reset functionality).
- The next 14 bytes contain optional customized factory data. The customized factory data bytes are factory programmed.

Refer to the N25Q 256Mb data sheet for more information.

Table 13: Read Identification Summary

Parameter	N25Q Code	S25FL Code
Manufacturer ID	20h	01h
Memory type	BAh	02h
Memory capacity	19h (256Mb)	19h

Reset

The RESET function restores the device to its initial power-up state.

The S25FL has an additional pin on SOIC-16, TBGA24, and FAC024 packages that functions as hardware reset. The N25Q device has a hardware RESET pin as an alternative to the HOLD pin on all packages, on dedicated part numbers. A software RESET command is available on both devices (see the Command Set table for an opcodes comparison).

After a RESET operation, the S25FL is always in 3-byte address mode, with the dummy clock cycles and quad I/O protocol enable/disable defined by registers. Depending on the state in configuration register 2, BP bits may be volatile or nonvolatile. The N25Q is defined by the nonvolatile configuration register content after a RESET and can be customized for the address mode as well.

Conclusion

Comparing the features of the Micron N25Q 256Mb and the Spansion S25FL Flash memory devices enables users to migrate applications from the S25FL to the N25Q 256Mb device.



Revision History

Rev. B – 4/12

- Added cross-references for 4-byte clarification to the Command Set table in Commands

Rev. A – 12/11

- Initial release

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